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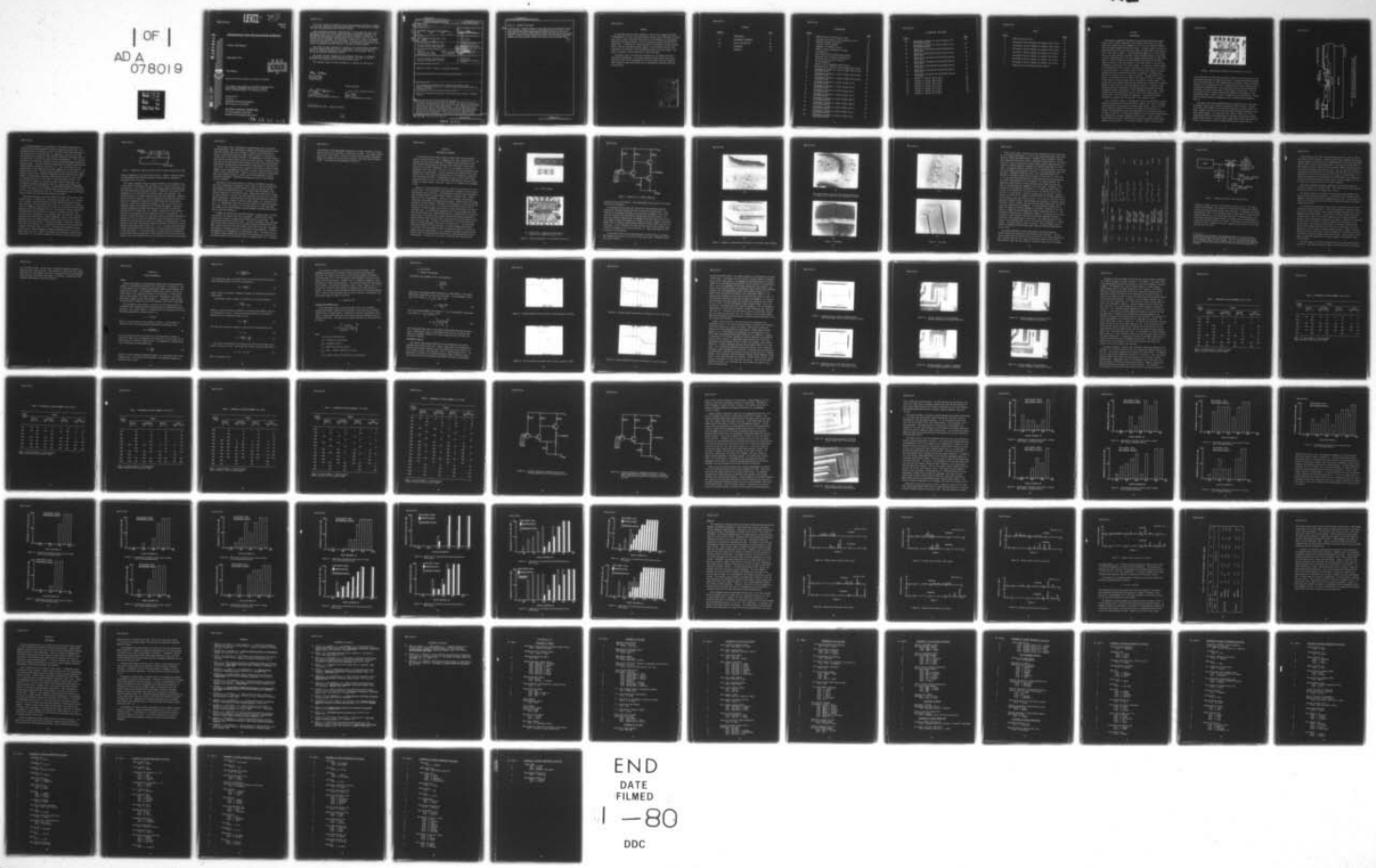

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MICROCRACKS AND METALLIZATION BURNOUT

Armen E. Mardiguian

September 1979

Final Report

This research was sponsored by the Defense Nuclear Agency
under Subtask Z99QAXTB027, Work Unit 31, Transient
Radiation Response Models for Integrated Circuits.

Prepared for
Director
DEFENSE NUCLEAR AGENCY
Washington, DC 20305

AIR FORCE WEAPONS LABORATORY
Air Force Systems Command
Kirtland Air Force Base, NM 87117

This final report was prepared by the Air Force Weapons Laboratory, Kirtland Air Force Base, New Mexico, under Job Order WDNE1902. Lieutenant Marilyn McQuade (ELP) was the Laboratory Project Officer-in-Charge.

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

This report describes the work done to determine the extent to which the reliability of integrated circuits (ICs) suffers when those ICs contain small cracks (microcracks) in their metallization. It was hypothesized that microcracked devices would undergo metallization at lower current pulses than unmicrocracked devices. Six hundred triple three-input NAND gates manufactured by Texas Instruments were used, of which 300 had been deliberately processed to have microcracks. The devices were first examined under a scanning electron microscope and electrically characterized on the AFWL —> next page

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BLOCK 20. ABSTRACT (Concluded)

cont.

Fairchild 5000. Different batches of both cracked and uncracked devices were then subjected to pulses varying in pulse width from 10 ns to 500 ns. The short pulse widths assured approximately adiabatic conditions, for which development of a theory of metallization burnout (MBO) was relatively straightforward. Postpulse testing revealed that there is no significant difference between the levels at which cracked and uncracked devices underwent MBO.

PREFACE

Mr. Roe Maier and Capt James Ledbetter of the Air Force Weapons Laboratory, Electromagnetics Division, Transient Radiation Effects Branch (AFWL/ELP), provided many hours of useful discussion that helped lay the groundwork for experimental design and preliminary analysis. Much of the data was acquired by Amn Patricia Pape of ELP. In addition, Mr. Chuck Miglionico of the Materials Science Section, Physics Division, provided invaluable support in the scanning electron microscope work; Mr. Al Krause of ELP provided the optical microscope support. The author is grateful for the cooperation of these individuals.

The devices used in this work were purchased for the program from Texas Instruments Incorporated. The stresses endured by these devices were far outside the stresses of the environment for which they were designed; therefore, their showing in these tests should not be interpreted to mean that they were of poor quality.

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SECTION I

INTRODUCTION

Semiconductor components fabricated using the planar technology commonly employ a layer of metal, deposited on the surface of the device, for interconnections between the active elements on a chip, and for connection between input and output elements and lead wire bonds. The metal, usually aluminum, is vacuum deposited on the chip and is then etched to form a metallization pattern such as that seen in Figure 1. The metallization appears as the light shaded areas on the dark pattern of the chip. Before the metallization is deposited, a typical integrated circuit (IC) chip undergoes several processing steps which produce a series of layers of silicon dioxide on the surface of the device. Steps are present in the oxide wherever it has been etched to allow diffusion of dopants to create part of an active element. In addition, a contact window is cut through the oxide to allow for the electrical connection of the silicon to the metallization. The contact windows and oxide steps produce a varying topology over which the metallization must be deposited. A stylized cross section of a portion of an IC is shown in Figure 2. The metallization on an actual IC chip differs from that shown in the figure, in that it is usually thinner where it crosses an oxide step or the edge of a contact window. This construction in the metallization has been identified as a potential reliability problem for both ICs and discrete semiconductor devices. In addition, high current pulses can be generated in nuclear radiation environments by charge replacement currents, photocurrents, and electromagnetic pulse (EMP). These currents can cause metallization burnout of the IC by rapidly heating the aluminum until it melts and opens or evaporates. This potential nuclear vulnerability prompted the work described in this technical report.

Early reliability studies of semiconductor devices revealed several failure mechanisms associated with the metallization. Berger et al. (Ref. 1) examined these mechanisms as they applied to aluminum metallization. Failure was seen for the operating devices and devices stored under high temperature. In storage, high temperature stress caused degradation of the metallization over all parts of the chip. For operating components, failure occurred preferentially at locations where elevated temperatures were present. A high resolution thermal plotter was used to identify three types of locations at which these temperatures are present: (1) the inside corners of bends in metallization,

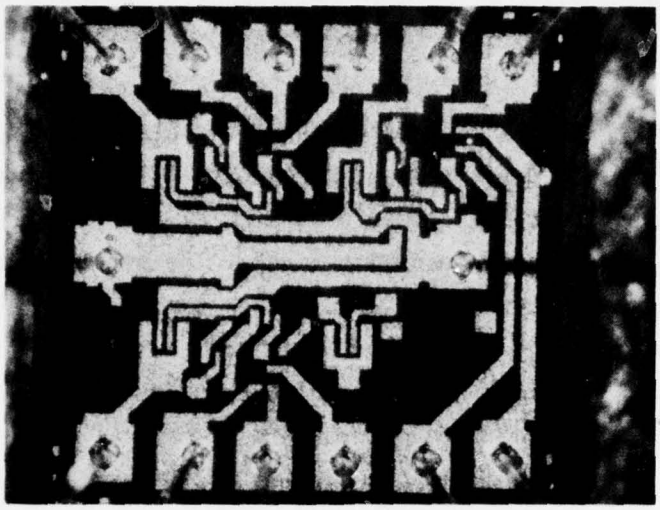


Figure 1. Metallization pattern on the surface of an IC chip.

(2) constructions at oxide steps and contact windows, and (3) over areas on the device where high power dissipation takes place. Failure mechanisms corresponding to the high ambient or local temperatures were primarily linked to chemical processes such as aluminum-silicon or aluminum-silicon dioxide reactions (Ref. 2). In addition, electromigration of the metallization under high current density conditions was found to cause opens in metallization stripes (Refs. 2 and 3). This process also was shown to proceed more rapidly at constructions of the metallization (Refs. 2 and 4), where it tended to be self-accelerating. Further studies of metallization on integrated circuits confirmed these mechanisms (Ref. 5).

Since many of the failure mechanisms were associated with the oxide steps and contact windows, much research was devoted to these locations. Optical microscopy was not capable of the resolution necessary to closely examine the steps. However, the angle of the step should be an important parameter in the metallization process. For steps which were "gently" sloped (e.g., 45°), a single metallization source perpendicular to the wafer surface should achieve adequate metallization. For more steeply sloped steps, uniform coverage of the sides of the steps would require multiple metallization sources (Ref. 4).

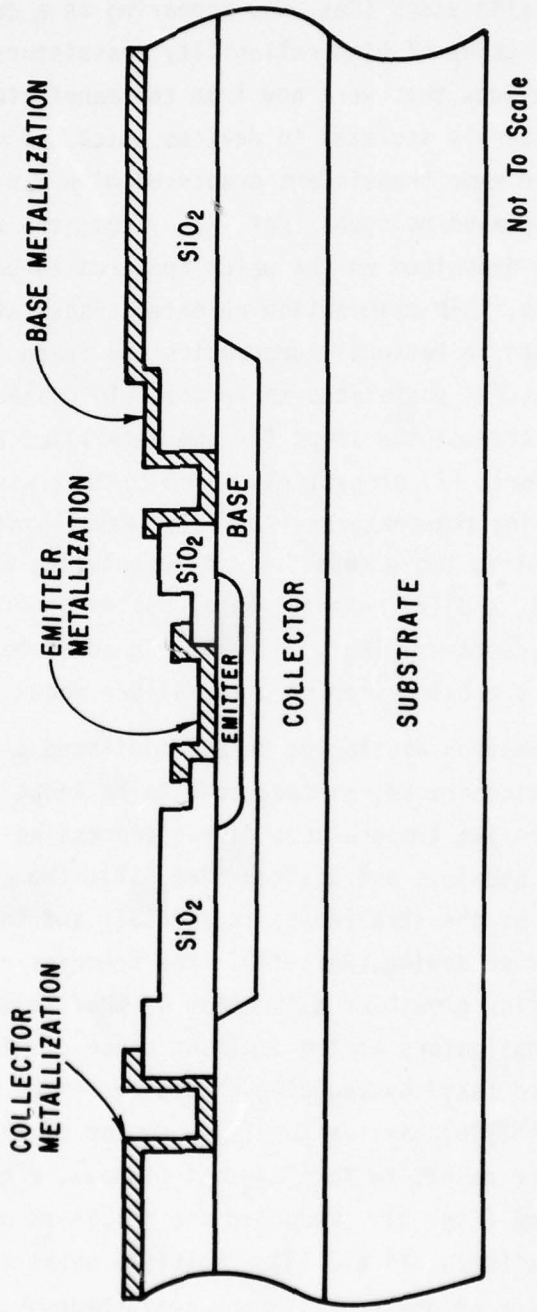


Figure 2. Stylized cross section of one transistor on an IC; emitter metallization runs perpendicular to page; base and collector metallization is in plane of page.

A significant advance in the evaluation of the problem was made when a scanning electron microscope (SEM) was used to examine the oxide steps. The increased resolution and depth of field of the SEM revealed electrical opens in the aluminum at the oxide steps (Ref. 6), appearing as a crack at the steps. Failure analysis of a group of high reliability transistors indicated cracks at the oxide steps in devices that were new from the manufacturer. Thus, the step problem was not necessarily isolated to devices which had undergone operating or storage stresses. The same transistors processed with a different metallization etching procedure displayed no opens (Ref. 7). Thus, the processing of the aluminum after it was deposited on the wafer appeared to be a determinant of the presence of the cracks. SEM examination revealed cracks at oxide steps in some commercial devices used in National Aeronautics and Space Administration (NASA) systems. The manufacturer postulated three possible causes for these cracks: (1) shadowing of the side of the steps (if the metallization source is not directly over the wafer), (2) excessively sharp contact window edges, and (3) excessive processing temperatures (Ref. 8). Metallization failure modes had appeared to fall into two groups: (1) manufacturing defects (undercutting of metal, thin metal), and (2) inherent metal system problems (electromigration, Al-Si or Al-SiO_2 interactions) (Ref. 9). The SEM added more detail and further defined the basis of the oxide step-related failure modes.

Despite the information available, debate continued as to the cause of the aluminum cracks, or microcracks, as they came to be known (Ref. 10). Explanations included: excessive temperatures during processing (sintering) cause over-alloying of the aluminum and silicon (Ref. 11); the profile of the oxide results in shadowing of the step (Refs. 12 and 13); and the metallization growth mechanism causes self-shadowing (Ref. 14). The theories related to deposition (including metallization growth as a function of profile) eventually were accepted by most investigators as the dominant cause of microcracks. Several solutions were offered based on reducing shadowing. Many IC chips employed a phosphosilicate glass (PSG) passivation layer on top of the silicon dioxide. When these layers were etched to form contact windows, a negatively sloped profile could be produced (Fig. 3). Reducing the thickness of the PSG would help eliminate microcracks (Refs. 14 and 15). Multiple metal evaporation sources could be used to reduce shadowing, although self-shadowing could still take place (Refs. 15 and 16). Models and computer codes developed to examine these effects (Refs. 17, 18, and 19) revealed the microcracks could grow even under

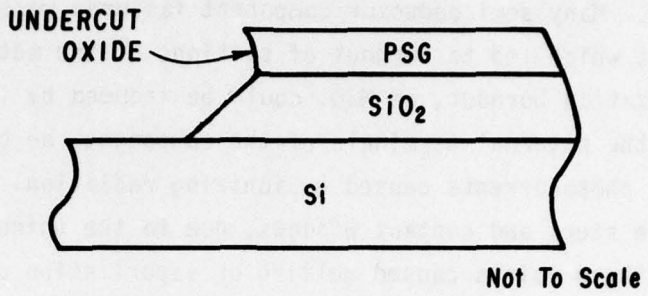


Figure 3. Negatively sloped oxide profile due to slower etching rate of PSG.

optimum arrangements of the metallization sources. However, substrate heating (to approximately 300°C) during evaporation could reduce the incidence of microcracks (Refs. 14 and 15).

While these procedures offered increased reliability, the presence of even a small number of microcracks was considered to be a reliability problem. This was especially so for military systems, which operate under extreme conditions which may exceed normal design specifications. Production line testing of all components, or of a statistically significant sample, was advocated. Two possible methods for screening against microcracks were postulated: electrical overstress and SEM inspection. Selective production line sample-screening by SEM was first proposed by researchers at NASA Goddard Space Flight Center (Ref. 20). Sampling and inspection techniques, as well as criteria and lot acceptance methods, were proposed for use in NASA procurements. Many semiconductor manufacturers adopted SEM inspection, and an SEM test method was prepared in MIL-STD format (Ref. 21). However, objections to SEM inspection were raised, most dealing with the subjective nature of the evaluation. In addition, surface coverings on IC chips (such as glass passivation) modified the appearance of the chip, obscuring information from SEM inspection (Ref. 22). Current pulse testing would not suffer this problem of interpretation of results. Autonetics Division of North American Rockwell developed a current pulse test to determine metallization quality (Ref. 23). A 5 A, 1 μs square pulse was passed through a metallization stripe covering at least two oxide steps and containing at least two corners. If the stripe failed, all metallization was etched off, and new metallization was deposited. While supplier yield and reliability were improved, some doubt remained about the test's ability to screen out microcracks.

High current pulses, unfortunately, represented more than a microcrack testing procedure. Many semiconductor component failures were found to result from high currents which led to burnout of sections of the metallization pattern. Metallization burnout, or MBO, could be induced by injection of a current pulse at the external terminals of the component, or by charge replacement currents and photocurrents caused by ionizing radiation. Burnout was often localized to oxide steps and contact windows, due to the thinner metallization. Joule heating of these points caused melting or vaporization of the metallization stripe. This failure mode was of concern to the nuclear radiation effects community since electromagnetic pulse (EMP) or nuclear ionizing radiation could produce currents leading to MBO. Research at several laboratories (among them: AFWL, Harry Diamond Laboratory, Boeing, and IRT) confirmed MBO in nuclear radiation environments. Mechanisms of burnout and sources of the currents were also examined.

Realization of thin metallization as a nuclear vulnerability resulted in work which supplemented the commercial effort either to improve the metallization coverage or develop effective methods to screen out devices with poor metallization (including microcracks). The method under development at the time was inspection of chips using the SEM. Though some current pulse testing had been performed, it was not clear that these tests could be used as a screen against microcracks. The SEM was thus the best available method for examining device metallization, though it suffered in some respects as a production line tool: (1) SEM operators would have to be well trained to recognize microcracks; (2) it was a fairly slow process; (3) not every device, nor even every wafer was tested; and (4) some microcracks occurred beneath the surface and would not show up under SEM examination.

To examine the current pulse and SEM techniques in greater detail, the AFWL let contracts with Motorola and Texas Instruments. The objective of these efforts was to develop a current pulse screening test for microcracks. The experiments produced conflicting results. The Texas Instruments study concluded that current pulse testing was not an acceptable screening technique (Ref. 24). Most stripes failed over the oxide surface, rather than at the step. No bimodal distribution of burnouts was found as a function of pulse amplitude. Therefore, SEM examination was recommended on a wafer-by-wafer basis. In contrast to this, the Motorola study concluded that the metallization coverage at a step could be accurately measured using the burnout time as a parameter (Ref. 25). To resolve

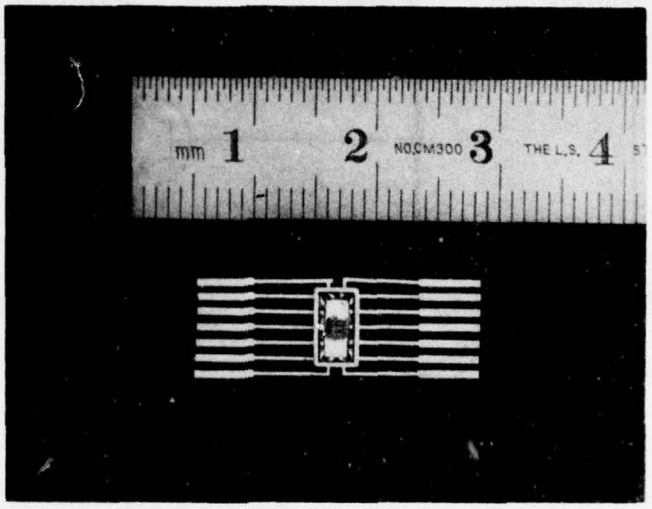
the difference in the experimental conclusions, the AFWL initiated an in-house effort to evaluate the potential of current pulse screens. This report presents the results of that effort. Section II discusses the experimental procedures; Section III presents the results and the analysis, which was based on theories of MBO. The conclusions are presented in Section IV.

SECTION II

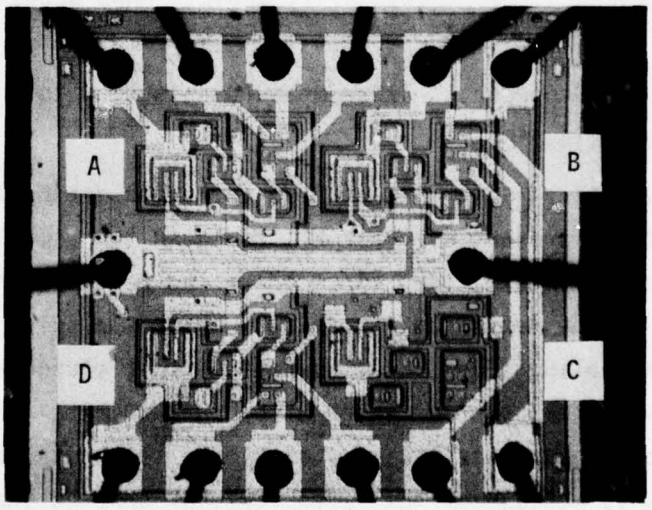
EXPERIMENTAL PROCEDURE

To characterize metallization burnout for both "good" and microcracked devices, the AFWL ordered a set of components from Texas Instruments (TI). Six hundred triple three-input NAND gates (TI SN54L10) were purchased, of which three hundred were processed so they would have microcracks at oxide steps. Figure 4a is an optical photograph of the IC in its package; Figure 4b is a photograph of the chip itself. The use of an IC for the tests presented unique advantages and disadvantages. Previous experiments had employed special test stripes; the IC tests were more representative of the conditions a production line screen would encounter. Disadvantages included multiple current paths through the device, as well as the presence of semiconductor junctions (either forward or reverse biased) in the path. Figure 5 is a schematic of the SN54L10 circuit.

Several ICs, with and without microcracks, were first examined with a mini-SEM and a SEM. This SEM examination was performed to attempt to locate specific microcracked steps on the chips. SEM photographs provided by Texas Instruments show microcracks where the metallization crossed a collector step. Figure 6 shows six of the TI photographs: Figures 6a-c are examples of microcracks; Figures 6d-f are examples of adequate step coverage. SEM and optical microscope examination at AFWL revealed a difference in the appearance of the metallization between the two sets of chips. The outline of the contact windows could be discerned on the microcracked chips, while no visible outlines were seen on the uncracked chips. This observation suggested that the microcracked chips might have been fabricated using thinner metallization; a second possibility--that the mask set used for forming contact windows had been deliberately misaligned to produce undercut oxide--was less likely since the outline of the window could be seen on all four sides. Estimates of the thickness of the metallization were based on the SEM photographs, with about ±10 percent error. The microcracked chip metallization over field oxide (not at a step) averaged approximately 1.4 μm thick, while the average thickness of the metallization on the unmicrocracked chips was approximately 1.9 μm. Although an appropriate correction was included, there was some additional uncertainty in these approximations due to viewing angle. In addition, the thickness as measured from several devices



(a) TI 54L10 package.



(b) TI 54L10 chip. (Quadrants of the chip are labeled A-D, clockwise from upper left.)

Figure 4. Optical photographs of the package and the chip.

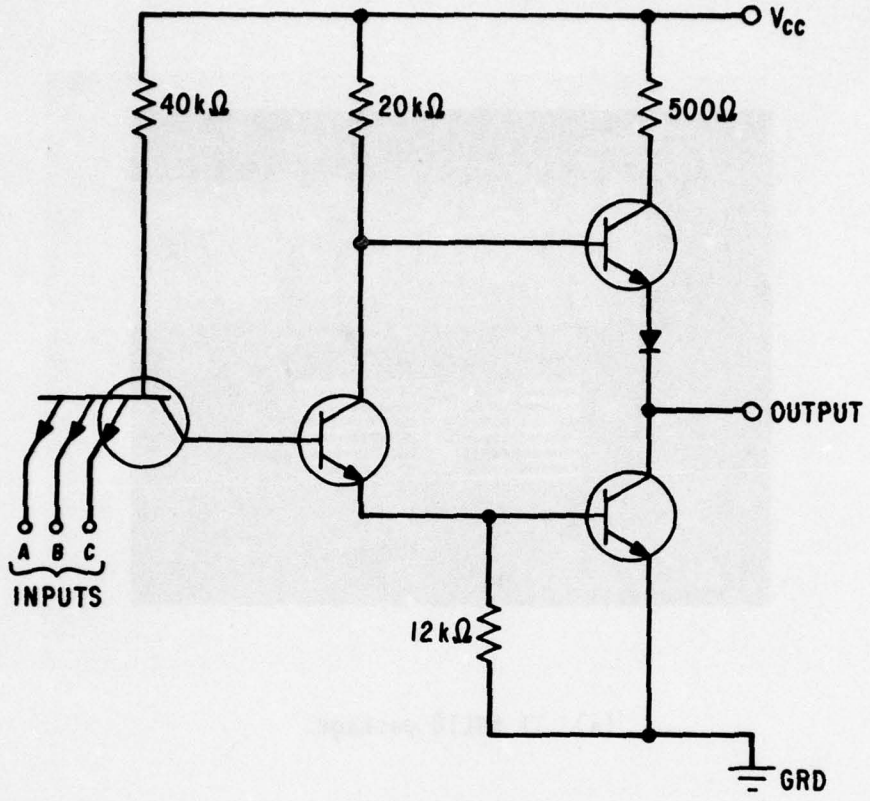
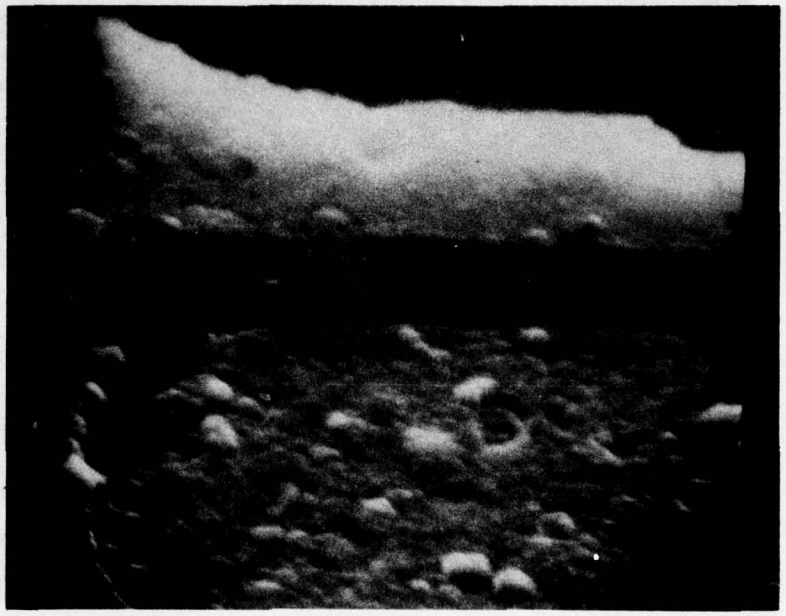


Figure 5. Schematic of TI SN54L10 NAND gate.

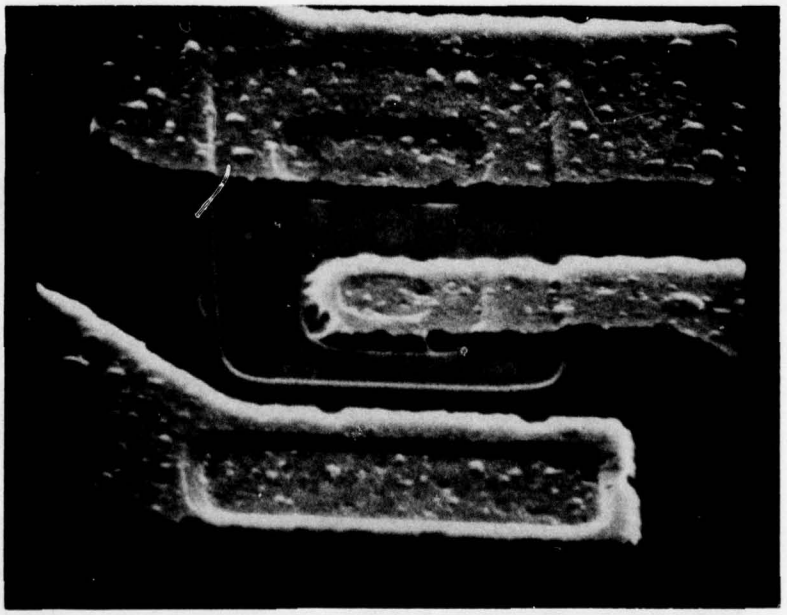
varied by as much as 20 percent. These measurements tend to confirm the thinner metallization hypothesis.

Few unambiguous microcracks were seen on the chips during the AFWL SEM examination, and those present were not all found in the same location. This affected the planned pulse testing, since there was no guarantee that a microcrack was located in the metallization through which the pulse passed. The tests were therefore planned under the assumption that microcracks were distributed randomly between the numerous oxide steps on the chip. However, the contact window steps for collector metallization should be the most likely locations for microcracks. This is because of the large vertical drop at these windows, equal to the full thickness of the field oxide (Fig. 2). Other oxide steps fall only a portion of that thickness.

To electrically test the ICs before and after current pulsing, an automatic test program was written for the Fairchild 5000 test system. Parameters tested are listed in Table 1.

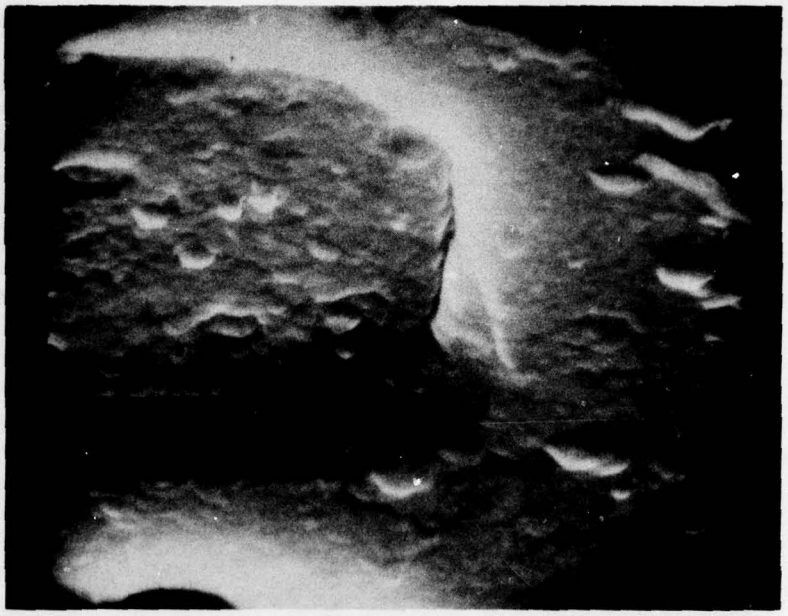


(a)



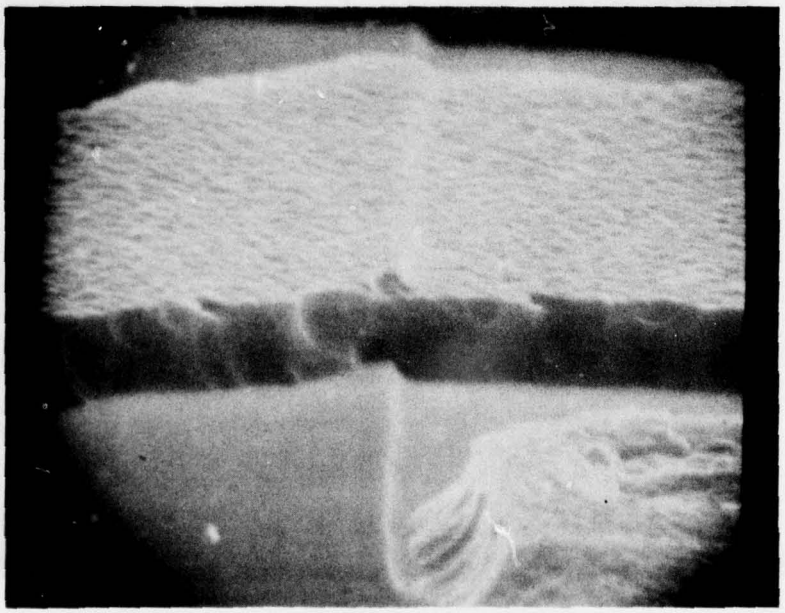
(b)

Figure 6. Examples of metallization microcracks at collector contact windows.



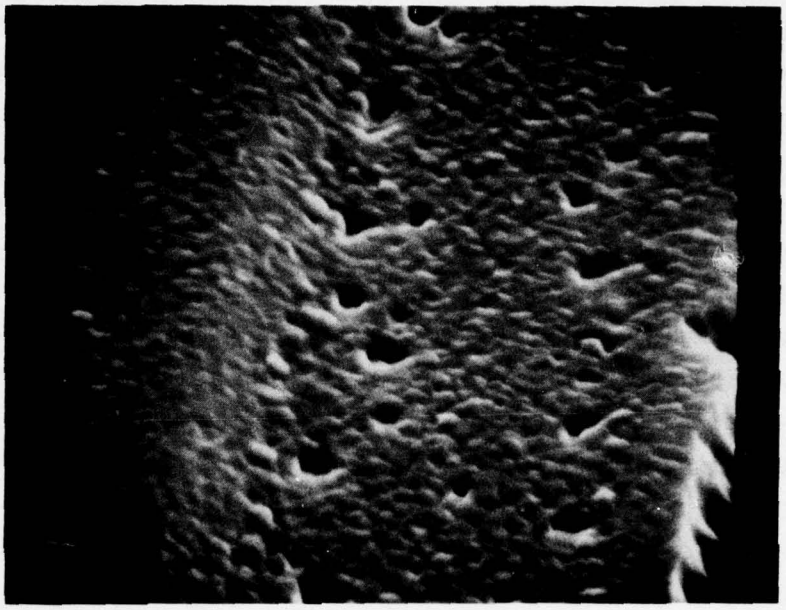
(c)

(This metallization crack over the collector oxide step is typical of all circuits in the cracked metal group.)



(d)

Figure 6. Continued.



(e)

(f)

Figure 6. Concluded.

Previous tests (Refs. 24 and 25) had been conducted with pulse widths from 50 ns to several microseconds. In the TI work, metallization over field oxide burned out before step metallization. Arguments based on adiabatic heating were proposed to explain this effect. According to these theories, the metallization at a step, or especially a contact window, would be heat-sunk more efficiently by the chip substrate, compared to the metallization over the field oxide. To approach adiabatic conditions for the step metallization, a narrower pulse with rapid rise-time would be necessary. The pulse generator chosen for this work, a BDM Model SN/SPG-200, used a set of open-ended delay lines (Blumlein) to produce variable duration pulses of up to 12.5 kV. Pulses had a 1 ns rise-time when operating into a 50 ohm load, and could be adjusted for 10 to 1000 ns pulsewidths in 10 ns increments. For proper operation, the experiment should present a 50 ohm resistance to the output of the pulser, equal to the characteristic impednace of the delay lines. Therefore, the IC resistance was an important consideration. If it were less than 50 ohms, a resistor of the appropriate value would have to be connected in series with the IC; if it were greater, a parallel resistor would be required. From an analysis of the IC circuit diagram, the resistance of the IC would probably be in each range at some time during the pulse. At the start of the pulse, the IC path would include at least a reverse-biased p-n junction or a diffused resistor (500 ohms or more). However, this junction would most likely break down during the pulse, presenting a low impedance. If the metallization opened, the IC might then present an infinite impedance to the pulser. Because of these conditions, a special 50 ohm terminator was placed in parallel with the IC. The experimental setup was thus a compromise, leading to a distortion of the pulses. In practice, some ringing of the pulse was observed, sometimes including a reflection at the ground point of the circuit. The voltage and current were measured at the selected input to the IC using precision resistors in a sealed coupler. The pulser setup is shown in Figure 7. The oscilloscopes used to record the voltage and current pulses were Tektronix R7704s with appropriate plug-in units.

The output transistors of the IC were chosen for the pulse testing. Positive pulses were injected at the collector of the transistor. The most likely current path was through the base and emitter of the output transistor to the IC ground, which was also chosen as the ground connection for the tests. While parallel paths did exist, they all involved at least the 12 kΩ resistor

TABLE 1. SN54L10 PARAMETER TESTS

Test No.	Parameter	Test Condition	Minimum	Maximum
1-9	$V_{out(1)}$ - logical 1 output voltage	V_{cc} = 4.5 V V_{in} = 0.7 V, I_{out} = -100 μA	2.4 V	
10-12	$V_{out(0)}$ - logical 0 output voltage	V_{cc} = 4.5 V, V_{in} = 2 V I_{out} = 2 mA		0.3 V
13-21	$I_{in(0)}$ - logical 0 level input current (each input)	V_{cc} = 5.5 V, V_{in} = 0.3 V		
22-30	$I_{in(1)}$ - logical 1 level input current (each input)	V_{cc} = 5.5 V, V_{in} = 2.4 V		10 μA
31-39	$I_{in(1)}$ - logical 1 level input current (each input)	V_{cc} = 5.5 V, V_{in} = 5.5 V		100 μA
40-42	I_{os} - short circuit output current	V_{cc} = 5.5 V, V_{in} = V_{out} = 0	-3 mA	-15 mA
43	$I_{cc(0)}$ - logical 0 level supply current (average per gate)	V_{cc} = 5.5 V, V_{in} = 5 V		0.51 mA
44	$I_{cc(1)}$ - logical 1 level supply current (average per gate)	V_{cc} = 5.5 V, V_{in} = 0		0.2 mA

Note: Negative currents indicate current flowing out of the device: positive currents flow into the device.

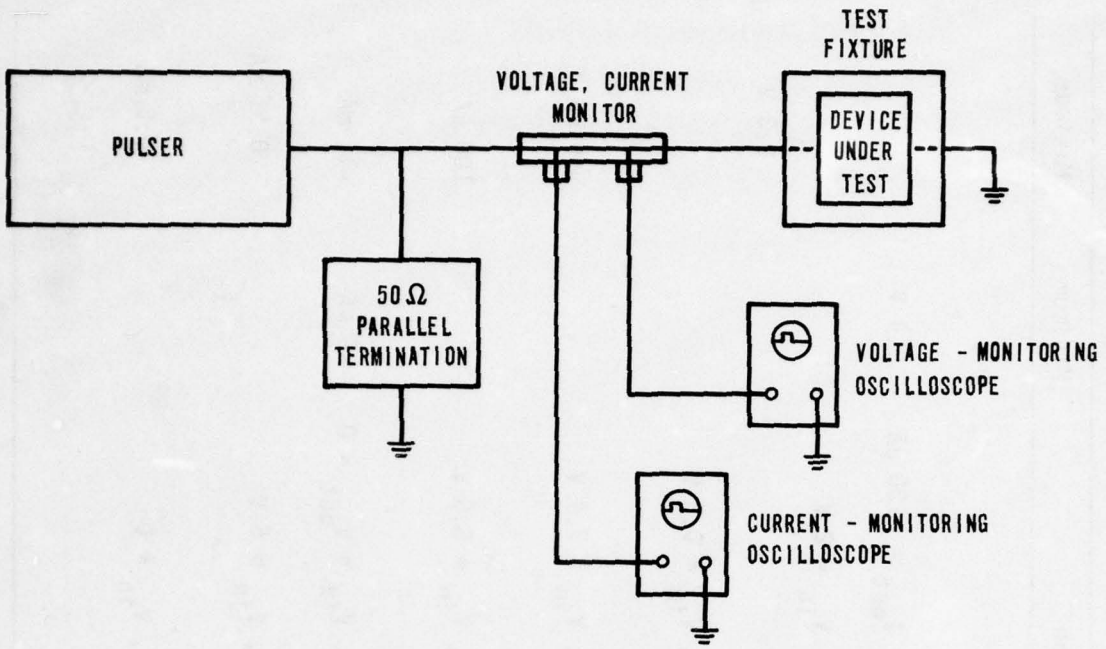


Figure 7. Apparatus used for current pulse testing.

between the emitter and base of the output transistor (Fig. 5). This represented a high impedance path compared to that directly through the transistor, assuming the reverse-biased junction would break down. In addition, the emitter metallization stripe, in its narrowest region, crossed four oxide steps and the contact window edge. Two of these steps were over a diffused resistor on the chip; these steps were probably formed at the same time as the base diffusion step, which the metallization also crossed. The fourth step was created by the emitter diffusion. Because of the chip's symmetry, gates D and A (Fig. 4) were both used for the tests.*

*A drawback to this method was the comparative widths of the collector and emitter metallizations--the collector metallization at the contact window was many times wider than the emitter stripe. Thus, if a microcrack were present at the collector window, and its thickness were less than the emitter metallization by the inverse of the width ratio, the microcrack would probably not be detected.

Pulse widths for this part of the experiment were 500 ns, 200 ns, 100 ns, 50 ns, 40 ns, 30 ns, and 20 ns. Some 10 ns pulses were attempted, but an unexplained problem in the pulser led to nonreproducibility of the pulse amplitude, and the results were not considered accurate. For each pulse width, devices were pulsed at a given voltage setting to determine whether they would burn out. Each device was tested at most once per gate. This was considered essential, since other investigators (Ref. 24) had found that step metallization could be improved after a pulse which melted but did not open the metallization. Six devices were tested at a given amplitude; the amplitude was then increased (or decreased) and another batch of devices tested. This was repeated until the 0 percent and 100 percent burnout levels were determined.

Each device underwent postpulse examination by optical microscope and electrical testing on the Fairchild 5000. These tests identified any damage to the metallization as well as damage to the silicon.

For several devices, the results of the electrical tests apparently disagreed with the microscope examination. These devices were retested using an ohmmeter to measure the resistance between the pulsed pins. In some cases, the device was also examined using the Mini-SEM to determine whether a microcrack failure had occurred.

The incidence of microcrack failures on two of the devices led to an additional set of current pulse tests. These were performed by injecting current at V_{CC} (pin 4) and providing a path to ground through the output (pin 5 or pin 3, depending on the gate pulsed). The current in this test divided into several alternate paths. Most of the current appeared to flow through the 500 ohm resistor, pull-up transistor, and diode to the output. Alternate paths included the 20 kΩ and 40 kΩ resistors. While it appeared that the majority of the current should flow through the 500 ohm path, it included a reverse-biased junction (the collector-base junction in the pull-up transistor), while the other paths did not include any reverse-biased junctions. However, the high voltage of the pulse should have caused a breakdown of the junction, providing the current a path only slightly larger than 500 ohms. Devices pulsed in this series of tests were examined by microscope, ohmmeter, and automatic tester after the pulse.

One final series of tests was performed using 10 ns pulses after repair of the pulser. The output transistor of gate B was pulsed, collector to emitter,

as in the first series. For this test, the 50 ohm termination resistor was placed in series with the device. This resulted in a pulse with less ringing and distortion. Microscopic, continuity, and electrical tests were performed before and after the devices were pulsed. In addition, some SEM tests were performed when anomalous results were present.

SECTION III

RESULTS AND ANALYSIS

THEORY

Several investigations of metallization burnout have included theoretical analyses of the heating and melting of the stripe (Refs. 23 through 27). Most of these analyses use an important simplifying assumption--that adiabatic conditions are in effect. This assumption requires that no heat be lost by the metallization to the underlying silicon or silicon dioxide. If the current pulse is short enough, this should be the case. Unfortunately, the various MBO reports disagree on what "short enough" is. In addition, oxide thickness and metallization thickness can affect the adiabatic time limit in some cases.

For the adiabatic case, heating is caused by the I^2R energy deposited in the metallization (neglecting other heat sources such as diffused resistors or junctions). For a given length, L, of metallization of cross-section A (in cm^2), the energy deposited by a constant current I is

$$E = (I^2RL/A)t \tag{1}$$

where R is the resistivity of the aluminum, in ohm-cm. If the current is a function of time, this relation must be rewritten in differential form:

$$dE = \frac{I^2(t)R(t)L}{A}\,dt \tag{2}$$

Here, R(t) indicates that the resistivity of the aluminum will change as a function of time, since the temperature and state (solid, liquid, vapor) of the metallization will change as heating occurs. The temperature of the metallization is related to the energy deposited:

$$dT = \frac{dE}{C\rho LA} \tag{3}$$

where dT is the differential temperature change, C is the specific heat of the aluminum, and ρ is the density of the aluminum. The temperature change as a function of time is thus

$$dT = \frac{I^2(t)R(t)}{C\rho A^2}\,dt \tag{4}$$

For a square wave pulse of constant current, the time and current required to reach the melting point are related by the equation

$$I^2t_1 = \frac{C\rho A^2\,\Delta T}{R} \tag{5}$$

where ΔT equals the change in temperature between the prepulse ambient and the melting point.

An additional amount of energy is required to melt the metallization:

$$E = \frac{I^2R_m tL}{A} = H\rho LA \tag{6}$$

where R_m is the resistivity of aluminum at its melting point (660°C), and H is the latent heat of fusion. The time and current necessary for melting the metallization (no temperature change) are then

$$I^2t_2 = \frac{H\rho A^2}{R_m} \tag{7}$$

The total time and current necessary to heat and melt the metallization are

$$t = t_1 + t_2 \tag{8}$$

$$I^2t = \frac{C\rho A^2\Delta T}{R} + \frac{H\rho A^2}{R_m} \tag{9}$$

Tasca (Ref. 27) performed the calculations for resistivity and heat capacitance as a function of time. The current-time relation after the substitions is

$$I = 1.95 \cdot 10^4\, At^{-\frac{1}{2}} \tag{10}$$

when A is measured in cm^2.

The resistivity, however, is a function of the film thickness. This dependence would require a different constant for each stripe thickness. Gurev (Ref. 25) found an almost exact inverse relation between the change in R and the change in I^2t. For his analyses, Gurev assumed a resistivity value based on the stripe thickness. However, this is a dangerous assumption since a microcrack will reduce stripe thickness. To avoid over-complicating the analyses in this report, the constant calculated by Tasca is used. However, even if the variation of resistivity with thickness is ignored, other complications are present. For example, further heating and vaporization of the aluminum probably occur. These will add additional terms to the I^2t relation. Nevertheless, the relation can always be stated in the form

$$I = (\text{constant})\ At^{-\frac{1}{2}} \tag{11}$$

assuming the adiabatic case.

In the nonadiabatic case, several additional factors are considered, including the thermal conductivity and thickness of the oxide and the thermal conductivity of the metallization. Reference 23 presents a nonadiabatic calculation. Another hybrid model was derived which treats both adiabatic and nonadiabatic conditions. The model yields a general equation for the current flow at failure.

$$I_f = W_m \left[\frac{T_{rf} X_m \bar{\sigma}_{T_{ok}}}{\bar{r}_m X_{ox} \left(1 - e^{-t_p/\tau}\right)} \right]^{1/2} \tag{12}$$

where

W_m = width of metallization

X_m = thickness of metallization

X_{ox} = thickness of oxide

T_{rf} = temperature rise for failure

$\bar{\sigma}_{T_{ox}}$ = average thermal conductivity of oxide

$\bar{r}_m$ = average electrical resistivity of metallization

t_p = pulse width

τ = thermal time constant

The thermal time constant in turn is calculated as

$$\tau = \frac{\overline{C}_{T_m} \rho X_m X_{ox}}{\overline{\sigma}_{T_{ox}}}$$

where C_{T_m} is the average thermal conductivity of metallization. This hybrid model can be simplified for short and long pulses. For the adiabatic (short pulse) case, where $t_p << \overline{\sigma}_{T_{ox}} / \overline{C}_{T_m} \rho X_m X_{ox}$, then

$$I_f = \frac{2.02 \cdot 10^4 A}{t_p^{\frac{1}{2}}} \tag{13}$$

This is in close agreement with Equation 10. For the nonadiabatic (long pulse) case, where $t_p >> \overline{\sigma}_{T_{ox}} / \overline{C}_{T_m} \rho X_m X_{ox}$, then

$$I_f = W_m \left[\frac{T_{rf} X_m \overline{\sigma}_{Tox}}{\overline{r}_m X_{ox}} \right]^{1/2} \tag{14}$$

This hybrid model thus covers a wide range of pulse widths and physical conditions. Unfortunately, many of the parameters necessary for the calculations have to be estimated, especially for actual devices for which the exact construction is unknown.

EXPERIMENTAL RESULTS

The original square waves produced by the pulse generator were greatly distorted by the device under test. Figure 8 shows copies of oscillographs of the pulse with no device present, and of the voltage and circuit traces for a test in which a 500-ns, 200-V pulse was used on a nonmicrocracked device. The distortion is a product of the impedance mismatch between the pulser charge line and the device, and the changes experienced by the device semiconductor

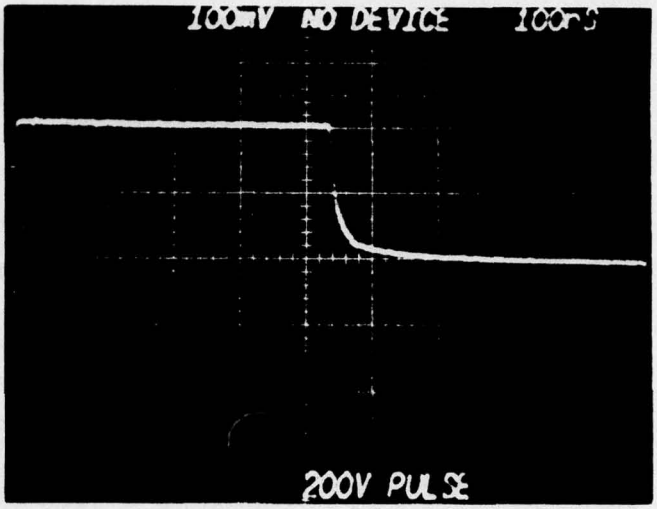


Figure 8a. Voltage waveform from pulser with no device present (100 V/cm).

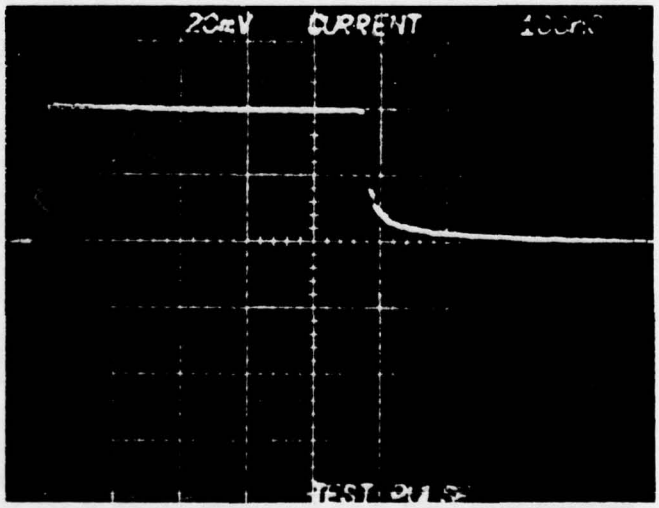


Figure 8b. Current waveform from pulser with no device present (2 A/cm).

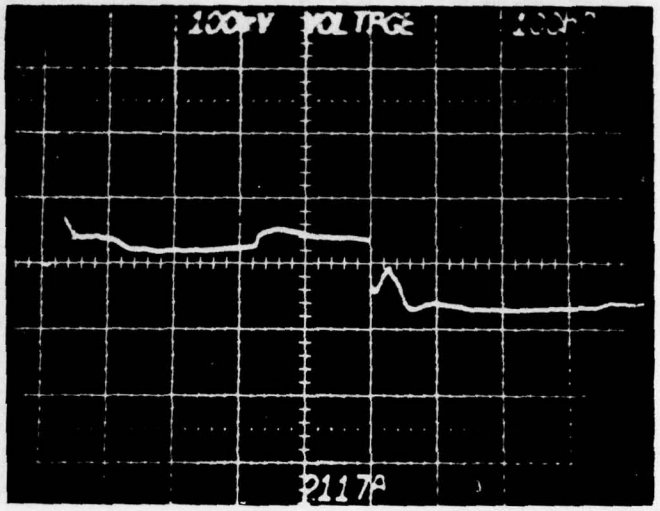


Figure 8c. Voltage waveform from pulser with device in circuit (100 V/cm).

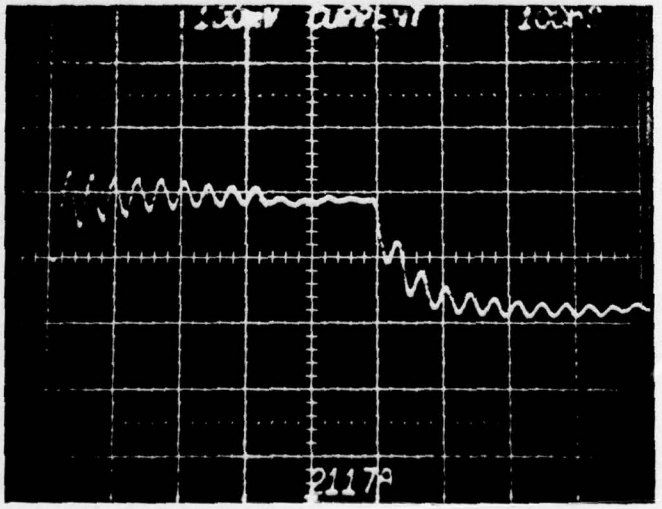


Figure 8d. Current waveform from pulser with device in circuit (10 A/cm).

junction and metallization. The primary features of the waveforms can be seen in the figure. The voltage (Fig. 8c) initially increases towards its maximum value (as set by the pulser). The impedance of the device during this time is largely due to the reverse-biased junction, and the current is correspondingly small. At a point dependent on the device construction, the voltage at the reverse-biased junction exceeds the breakdown voltage, and the device impedance assumes a low value approximately equal to the combined impedance of the metallization and the bulk resistance of the semiconductor material. The voltage across the device at this time is low, while the current is high. If the metallization melts (or vaporizes) and opens, the impedance of the device should approach very large values; the voltage will increase and the current will go to zero. For the oscillographs shown, no MBO occurred. Notice the presence of a reflection pulse due to the low impedance. For oscillographs of approximately 10 times the pulse duration, several reflections were sometimes seen (Fig. 9). In contrast, for those devices which do exhibit MBO, usually only one reflection was present (Fig. 10). However, the correlation between MBO and the waveforms was not good enough to predict burnout, especially as the pulse widths were decreased.

Damage to the devices fell into four qualitative categories, with appreciable overlap. The extent of damage generally increased with increasing voltage (or current) for a given pulse width. Some devices exhibited no measured electrical degradation or visual defects. Others showed junction damage (I) or a slight change in the appearance of the metallization (II). Still others had obviously melted metallization (III), or MBO (IV). Numbers in parentheses will be used to categorize failures; pictures corresponding to each are shown in Figure 11. MBO almost always occurred over field oxide, approximately halfway between points of larger cross-section or heat-sinking capability. Usually, supposedly identical pulses caused effects over a wide range. This variation was probably caused by two sources: pulser amplitude variations, and/or differences in the devices. Amplitude error was supposed to be approximately 1 percent, not enough to account for the variations in damage. However, since the devices did not represent a dynamic 50-ohm impedance, larger errors in pulse amplitude could have existed. The most likely source of variation was a combination of both the pulser and devices. While this did tend to scatter the results, it is a problem that would probably be present in any tests of actual devices.

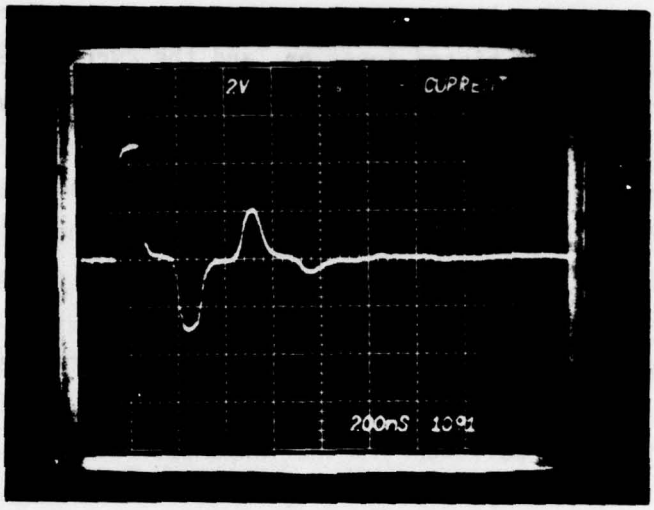


Figure 9. Distortion due to multiply reflected pulse; pulse width equals 100 ns; 5 A/cm vertical setting.

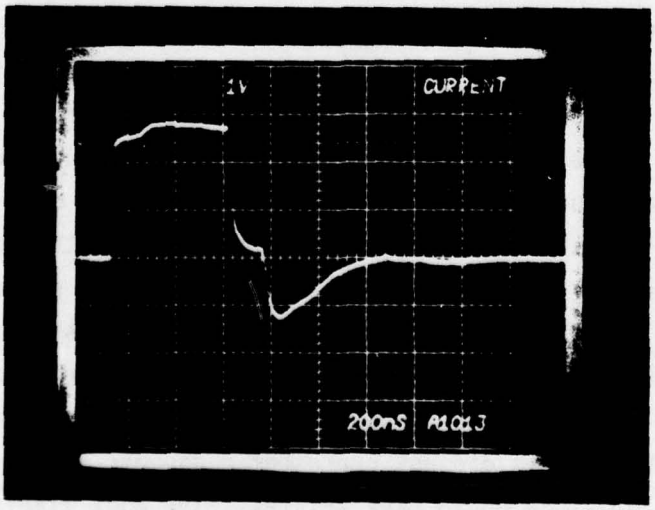


Figure 10. Distortion due to single reflection; pulse width equals 500 ns; 2.5 A/cm vertical axis.

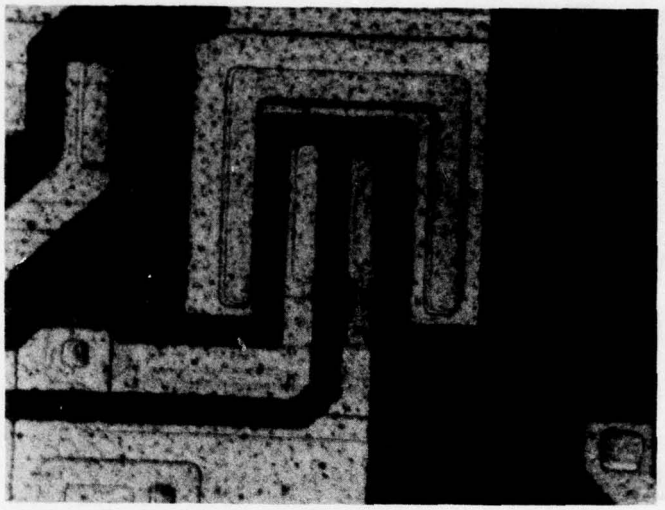


Figure 11a. Failure category I; arc-over between emitter and collector of output transistor.

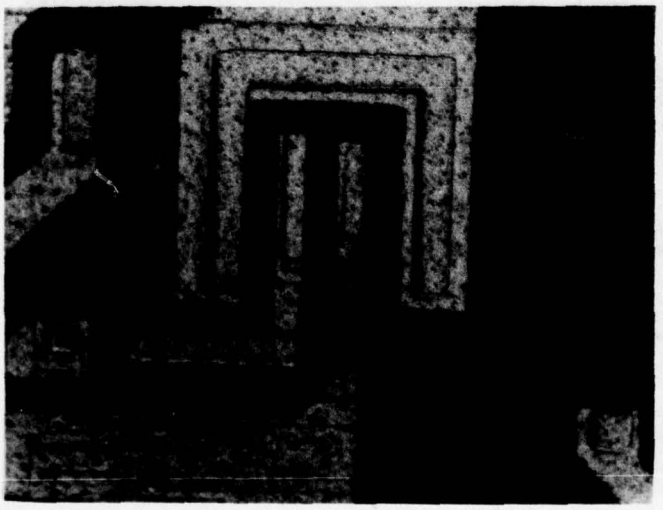


Figure 11b. Failure category II; change in appearance of emitter metallization due to heating.

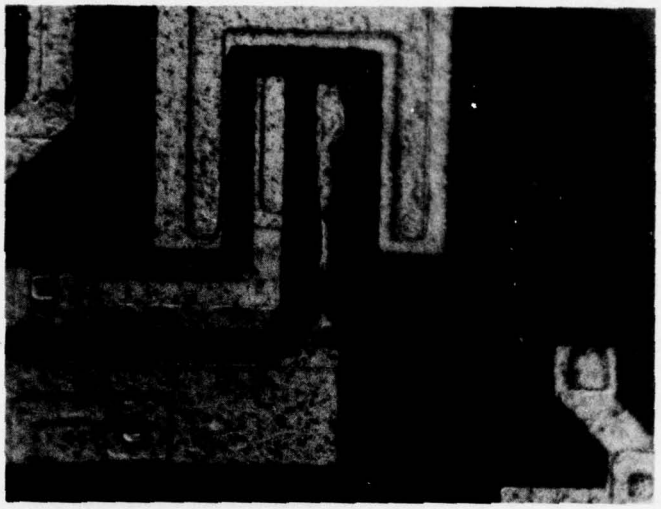


Figure 11c. Failure category III; obvious melting of emitter metallization stripe.

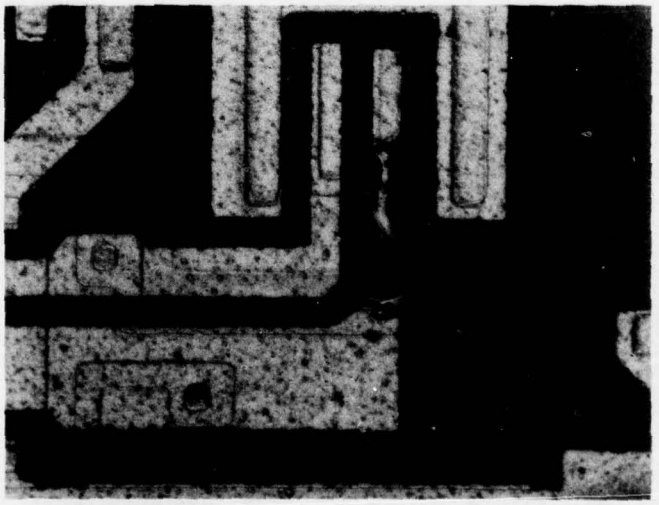


Figure 11d. Failure category IV; metallization burnout of emitter metallization stripe.

The types of failures, based on the electrical and microscopic examinations, are listed by category in Tables 2 through 8. The numbers in the tables refer to the percentage of devices that suffered at least as much damage as the given category. This assumes that a device showing damage in a higher category passed through each of the lower categories during the pulse. For example, a device with melted metallization had obviously progressed through the point where small changes had occurred in the appearance of the metallization; in addition, the electrical and resistance tests indicated that most melted devices had suffered junction damage. Variations in device damage thresholds can be seen in the slow increase from 0 to 100 percent over several voltage steps, as well as the nonmonotonic increases. Junction damage was usually visible as a dark spot (Fig. 11a) or spike connecting two or three regions of the output transistor. This indicated physical damage such as arc-over or melting of the silicon. In some cases, no visible damage was present but electrical failure had taken place. Electrical tests after pulsing confirmed damage to the junctions for most of those devices which did not suffer MBO. The junctions in these cases appeared as a resistance with no semiconducting character. The circuit then acted as shown in Figure 12a. The devices failed the test for high output voltage for any of the three inputs set low. If the resistance of the transistor was several hundred ohms, the device also failed the test for low output voltage (all three inputs high); when the resistance was below approximately 100 Ω, the device passed this test. For resistances of several thousand ohms or more, or in cases when MBO occurred, the devices usually failed only the low output voltage test. A separate test using a volt-ohmmeter showed that the collector-base junction was also damaged in these cases. The emitter-base junction could not be tested, since the emitter metallization burned out. However, this junction probably was destroyed.

In several instances, a device under microscopic examination appeared not to have MBO, but failed the electrical tests in a manner that suggested burnout had occurred. This anomaly appeared more frequently at shorter pulses. The ohmmeter tests of these devices assumed more importance in these cases, since they differentiated between actual opens and high resistances (on the order of several thousand ohms). Approximately half of the anomalous results were shown to be high resistances, indicating continuous metallization. However, some devices, both microcracked and uncracked, were found to be open. This indicated a possible open in the collector metallization (opens in the emitter would still

TABLE 2. PERCENTAGE OF DEVICES DAMAGED, 500 ns PULSE

Pulser Voltage (V)	Damage							
	Junction Burnout		Deformed Metallization		Obvious Melting		Open Metallization	
	M	U	M	U	M	U	M	U
100	100	-	0	-	0	-	0	-
140	100	-	83	-	17	-	0	-
150	-	100	-	100	-	50	-	50
160	-	100	-	100	-	50	-	33
170	-	100	-	100	-	67	-	33
180	100	100	100	83	100	33	67	17
190	-	100	-	100	-	100	-	33
200	100	100	100	100	100	100	100	100
220	100	-	100	-	100	-	100	-

Note: M = microcracked; U = unmicrocracked.
Dashes indicate no test at given voltage.

TABLE 3. PERCENTAGE OF DEVICES DAMAGED, 200 ns PULSE

Pulser Voltage (V)	Damage							
	Junction Burnout		Deformed Metallization		Obvious Melting		Open Metallization	
	M	U	M	U	M	U	M	U
200	100	100	83	83	33	83	0	0
220	-	100	-	67	-	67	-	0
240	100	100	100	100	100	67	17	33
260	100	100	100	100	100	100	100	67
280	100	100	100	100	100	100	100	50
300	-	100	-	100	-	100	-	100

Note: M = microcracked; U = unmicrocracked.
Dashes indicate no test at given voltage.

TABLE 4. PERCENTAGE OF DEVICES DAMAGED, 100 ns PULSE

Pulser Voltage (V)	Damage							
	Junction Burnout		Deformed Metallization		Obvious Melting		Open Metallization	
	M	U	M	U	M	U	M	U
300	100	100	67	67	17	33	0	0
340	100	100	100	100	100	100	17	50
360	-	100	-	100	-	83	-	17
380	100	100	100	100	100	100	33	50
400	100	100	100	100	100	100	83	100
420	100	100	100	100	100	100	100	83
440	100	100	100	100	100	100	100	100

Note: M = microcracked; U = unmicrocracked.
Dashes indicate no test at given voltage.

TABLE 5. PERCENTAGE OF DEVICES DAMAGED, 50 ns PULSE

Pulser Voltage (V)	Damage							
	Junction Burnout		Deformed Metallization		Obvious Melting		Open Metallization	
	M	U	M	U	M	U	M	U
420	-	100	-	17	-	17	-	17
440	-	100	-	40	-	40	-	40
460	-	100	-	67	-	50	-	50
480	-	100	-	100	-	83	-	67
500	100	100	100	100	50	83	17	83
520	-	100	-	100	-	83	-	17
540	100	100	100	100	100	83	50	83
560	100	-	100	-	100	-	83	-
580	100	100	100	100	100	100	100	100
600	100	100	100	100	100	100	100	100

Note: M = microcracked; U = unmicrocracked.
Dashes indicate no test at given voltage.

TABLE 6. PERCENTAGE OF DEVICES DAMAGED, 40 ns PULSE

Pulser Voltage (V)	Damage							
	Junction Burnout		Deformed Metallization		Obvious Melting		Open Metallization	
	M	U	M	U	M	U	M	U
460	-	83	-	33	-	33	-	0
480	-	100	-	83	-	83	-	67
500	-	100	-	83	-	83	-	83
520	100	100	33	83	17	83	0	83
540	100	100	67	100	33	100	17	83
560	100	100	100	100	50	100	33	50
580	100	100	100	100	100	83	83	83
600	100	100	100	100	100	100	50	100
620	100	100	100	100	100	100	83	100
640	100	-	100	-	100	-	100	-
660	100	-	100	-	100	-	100	-

Note: M = microcracked; U = unmicrocracked.
Dashes indicate no test at given voltage.

TABLE 7. PERCENTAGE OF DEVICES DAMAGED, 30 ns PULSE

Pulser Voltage (V)	Damage							
	Junction Burnout		Deformed Metallization		Obvious Melting		Open Metallization	
	M	U	M	U	M	U	M	U
500	-	67	-	33	-	33	-	17
540	-	83	-	50	-	50	-	33
560	83	-	83	-	33	-	0	-
580	-	100	-	67	-	67	-	67
600	100	-	100	-	67	-	33	-
620	-	100	-	83	-	50	-	33
640	100	-	100	-	83	-	67	-
660	100	100	100	67	100	67	83	33
680	100	-	100	-	100	-	83	-
700	100	-	100	-	100	-	100	-
720	100	100	100	100	100	83	100	67
740	-	100	-	100	-	100	-	67
760	-	100	-	100	-	100	-	100

Note: M = microcracked; U = unmicrocracked.
Dashes indicate no test at given voltage.

TABLE 8. PERCENTAGE OF DEVICES DAMAGED, 20 ns PULSE

Pulser Voltage (V)	Damage							
	Junction Burnout		Deformed Metallization		Obvious Melting		Open Metallization	
	M	U	M	U	M	U	M	U
700	100	83	33	33	0	0	0	0
740	-	100	-	50	-	50	-	50
780	-	100	-	67	-	50	-	33
800	100	-	100	-	67	-	0	-
820	-	100	-	50	-	50	-	50
840	100	-	100	-	83	-	33	-
860	-	100	-	67	-	67	-	67
800	100	-	100	-	83	-	33	-
900	100	100	100	100	100	67	83	33
920	100	-	100	-	100	-	100	-
940	100	83	100	83	100	83	100	67
960	100	-	100	-	100	-	100	-
980	100	100	100	100	100	100	100	83
1000	100	-	100	-	100	-	100	-
1020	-	100	-	83	-	83	-	83
1040	-	100	-	100	-	100	-	67
1060	-	100	-	100	-	100	-	100
1080	-	100	-	100	-	100	-	100

Note: M = microcracked; U = unmicrocracked.
Dashes indicate no test at given voltage.

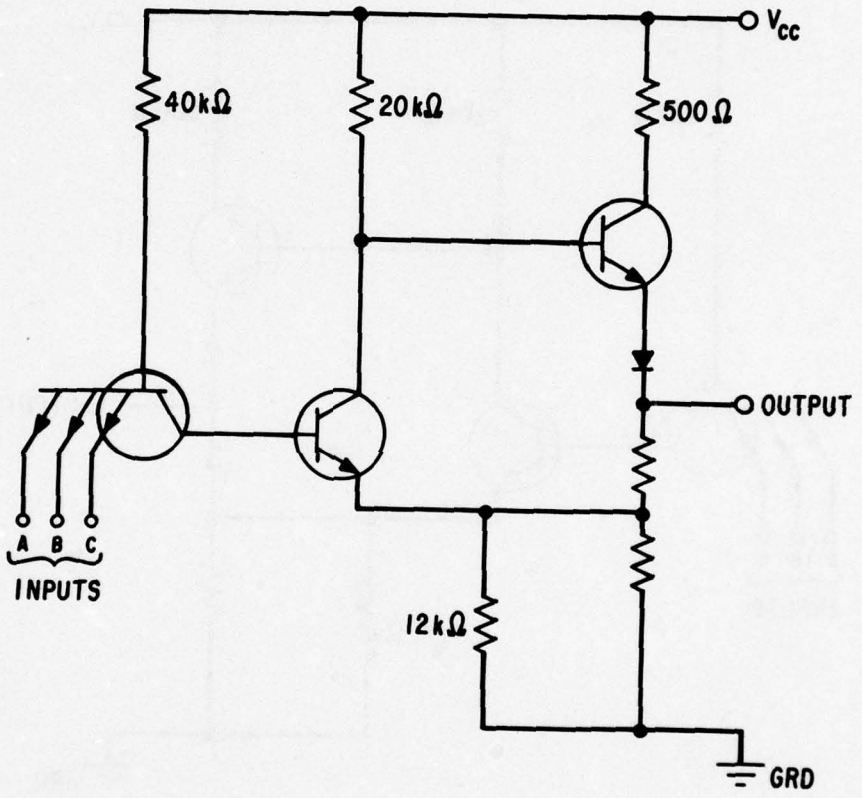


Figure 12a. Possible appearance of NAND gate after pulse testing; output transistor has become resistive.

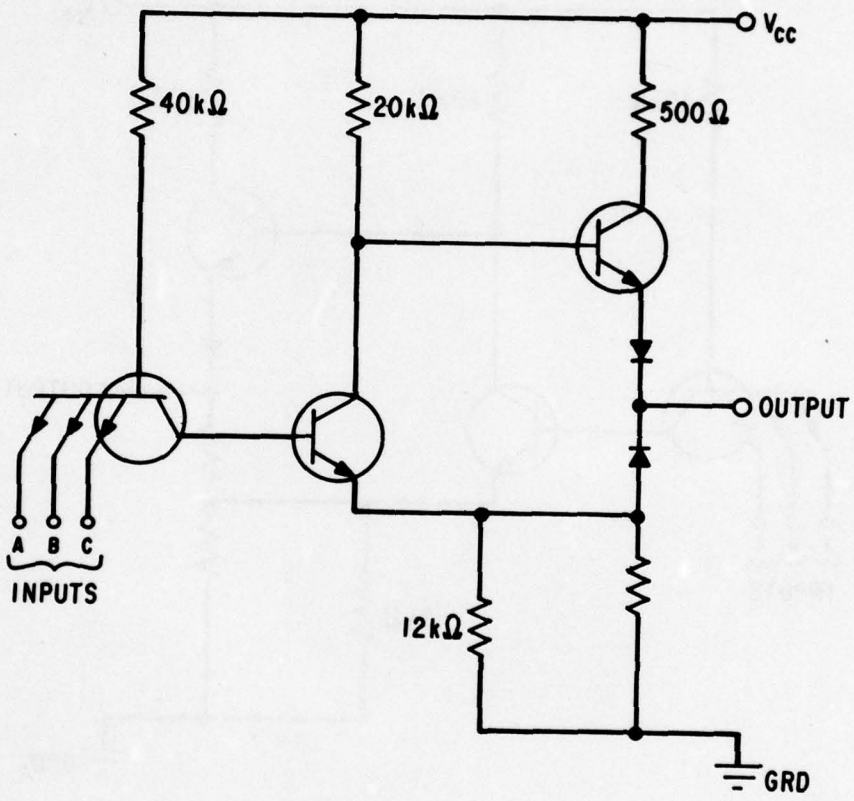


Figure 12b. Possible appearance of NAND gate after pulse testing; emitter-base junction of output transistor is resistive, while collector-base junction still maintains rectifying abilities.

allow current to pass through the 12 kΩ resistor). Damage categories for the anomalous results were assigned on the basis of these tests. Percentage of devices damaged, as shown in Tables 1 through 7, thus reflect the results of optical microscope examination, automatic electrical test, and ohmmeter continuity checks.

Anomalous devices electrically open were also examined using the SEM. For most of the anomalous devices, no cause could be found for the opens. Some uncracked devices showed pitted metallization at the edge of the contact window (Fig. 13a); whether these were opens was unclear. Other devices may have had broken leads or wire bonds, or opens in the semiconductor material. An additional electrical explanation for these devices could be a failed emitter-base junction, coupled with an undamaged collector-base junction. This type of junction damage is not likely--electrical overstress tests have shown that forward-biased junctions are less susceptible to permanent damage than reverse-biased junctions. In the tests reported here, the positive pulse was applied at the collector. Therefore, the collector-base junction of the n-pin output transistor was reverse-biased while the emitter-base junction was forward-biased. If the emitter-base junction nevertheless failed in the manner described above, the circuit might look like that shown in Figure 12b. A positive voltage at the collector would reverse-bias the collector-base junction, giving a high resistance. However, the transistor would not turn on when it should. To verify this failure mode, the probes in the ohmmeter test were reversed to apply a positive potential to the device ground. This should have, and did, result in a low resistance. Unfortunately, the same result was found for undamaged circuits, due to the junction-isolated construction of the devices. Therefore, this failure mode of the circuit could not be verified.

However, two of the microcracked devices displayed unambiguous microcracks in the collector metallization at the contact windows (Fig. 13b). These microcracks may have become opens due to the high current pulses. The important consideration in these cases was the relative cross sections of the emitter stripe and the collector metallization. If the thicknesses of both metallizations were identical, the collector would have at least 30 times the cross section of the emitter where each crosses an oxide step, due to the difference in the width of the metallization. Since the burnout current is proportional to the cross section of the metallization, the emitter stripe should have suffered MBO at a

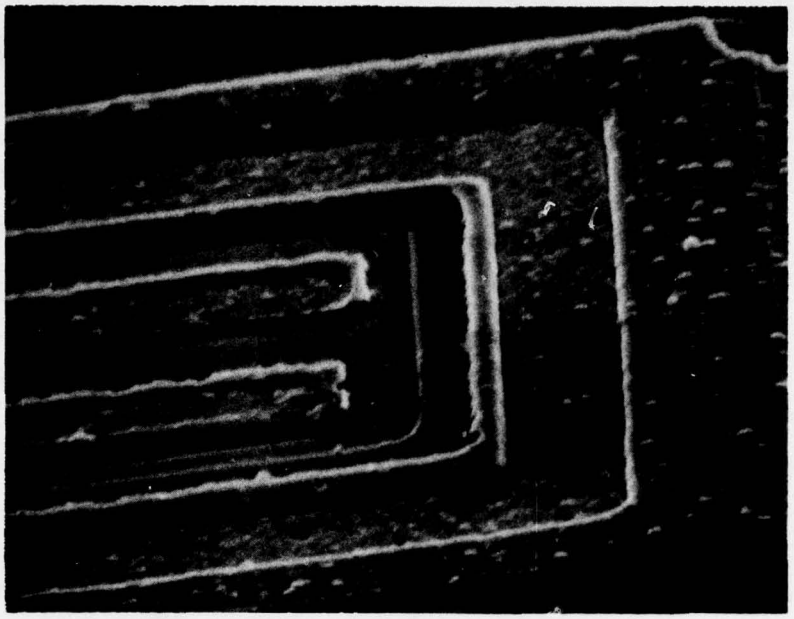


Figure 13a. Metallization microcrack at collector contact window after current pulsing.

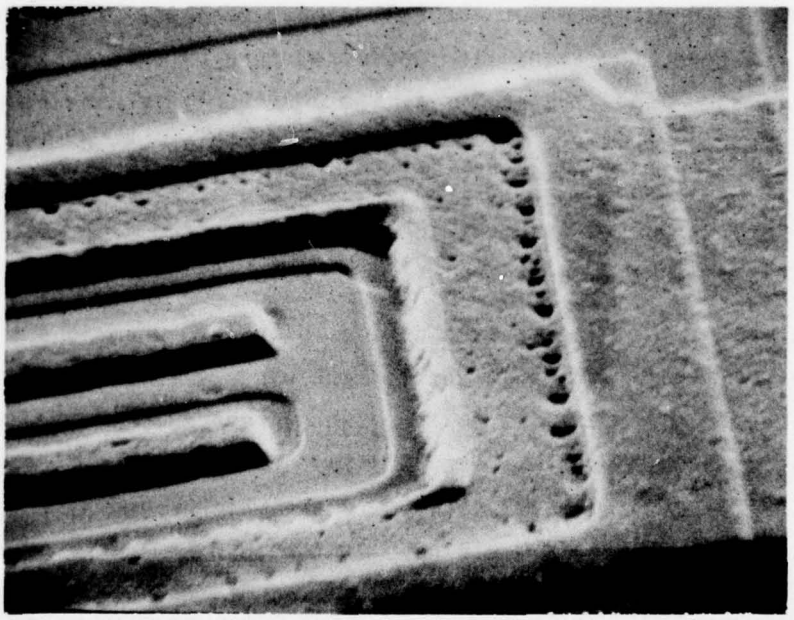


Figure 13b. Metallization pitting at collector contact window after current pulsing.

level 1/30th that of the collector. The fact that this was obviously not the case for at least these two anomalous devices indicated that the thickness of the collector metallization at the contact window step was less than 1/30th of the minimum emitter metallization thickness (assuming adiabatic conditions existed).

The large difference in thickness required between microcracked metallization at a collector step and otherwise "good" metallization indicated a possible shortcoming in the experimental procedure. If the collector microcrack were only 1/10 the thickness of the "good" metallization, it would not burn out in this experiment. The second series of current pulses was performed in an attempt to avoid the large difference in width between the collector metallization at the contact window and "good" metallization. If the widths were approximately the same, the microcracked metallization would burn out well before the uncracked metallization.

The second series of tests was performed using 10-ns pulses to minimize any effects caused by nonadiabatic conditions. The results were disappointing from an experimental point of view, primarily due to ambiguities in analysis of the electrical tests, and because of the multiple current paths through the circuit. In fact, all of the devices which suffered burnout did so at a narrow point in the collector metallization over the field oxide. There were no failures in which the ohmmeter tests disagreed with the microscope inspections. In addition, all of the devices showed degradation of the electrical parameters before any significant metallization change. The third series of tests was performed using the output transistor. These tests, also performed at 10 ns to help reduce heat loss from the crack region, yielded no clear differences in the voltage level that was required for burnout. For this pulse width, several devices which did not burn out did pass the electrical tests. There were also some anomalous results of the same nature as described earlier. Further modification of the experimental procedure was considered but abandoned, since other possible current paths suffered similar testing limitations (high series resistance, metallization paths over heat-producing areas, several parallel paths). The effects of these considerations on an assembly line screen are discussed later.

Returning to the original series of tests, Figures 14 through 20 are histograms showing percentage of MBO failures in unmicrocracked devices as a function of pulser voltage setting for each pulse width. The wide variation in burnout

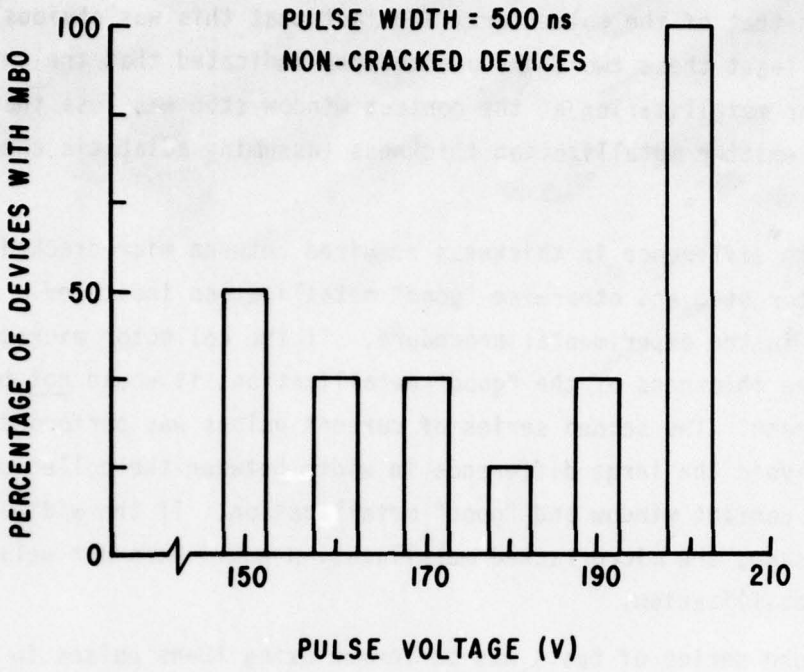


Figure 14. Percentage of burnouts versus pulser voltage, 500 ns pulse, uncracked devices.

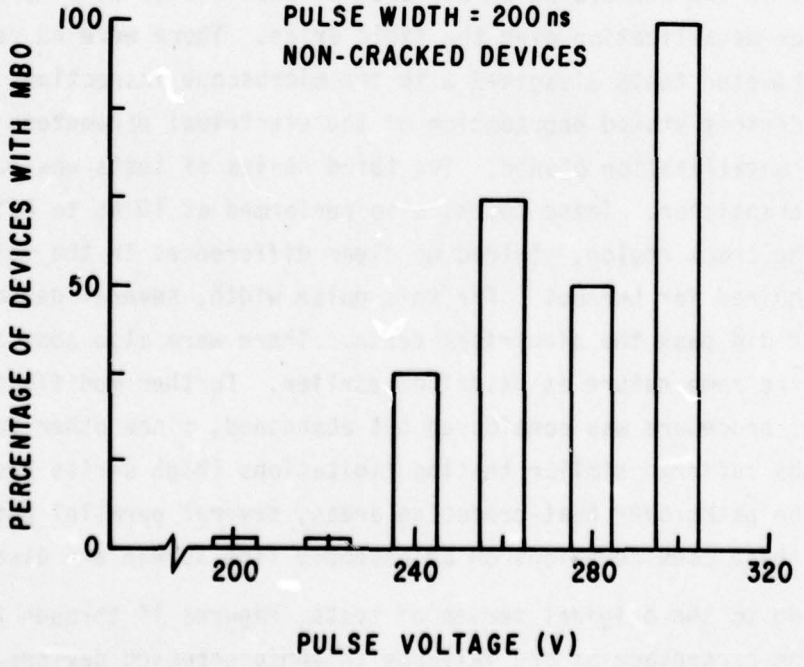


Figure 15. Percentage of burnouts versus pulser voltage, 200 ns pulse, uncracked devices.

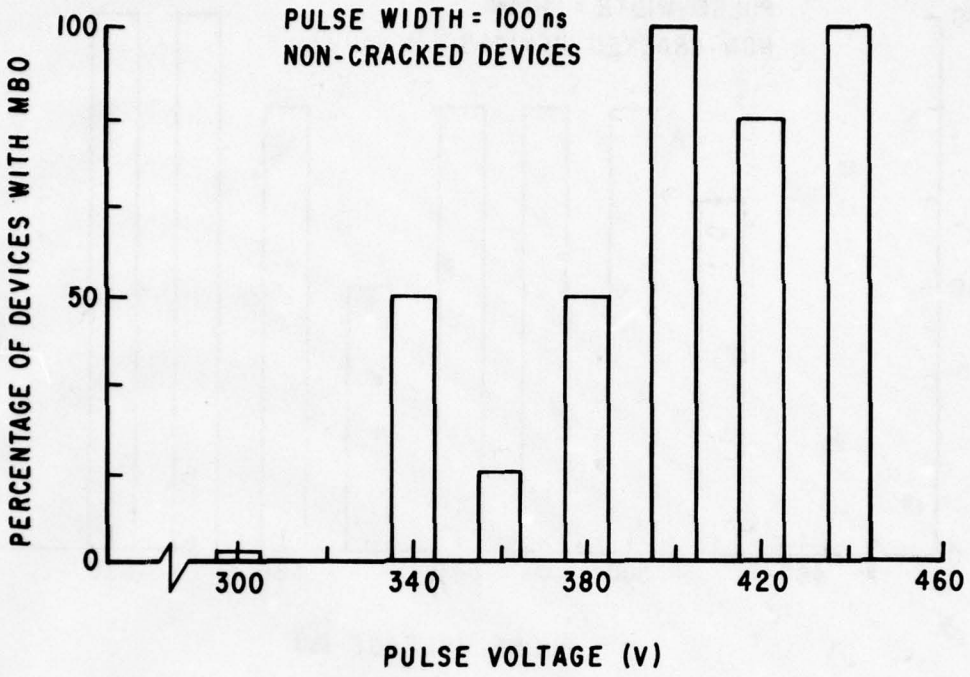


Figure 16. Percentage of burnouts versus pulser voltage, 100 ns pulse, uncracked devices.

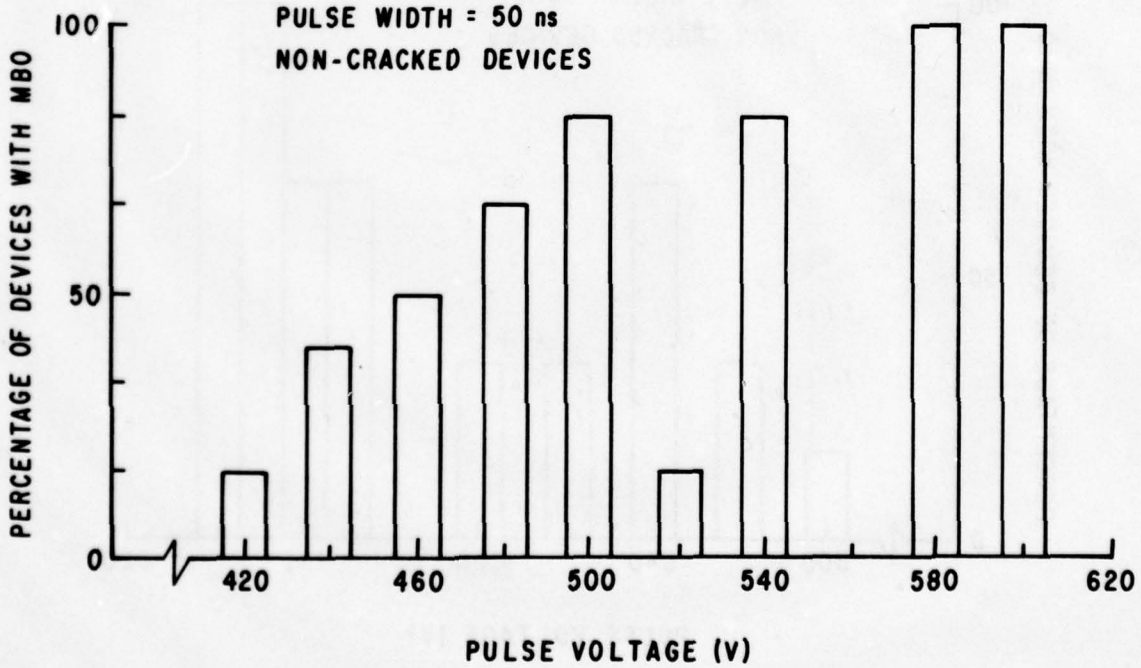


Figure 17. Percentage of burnouts versus pulser voltage, 50 ns, uncracked devices.

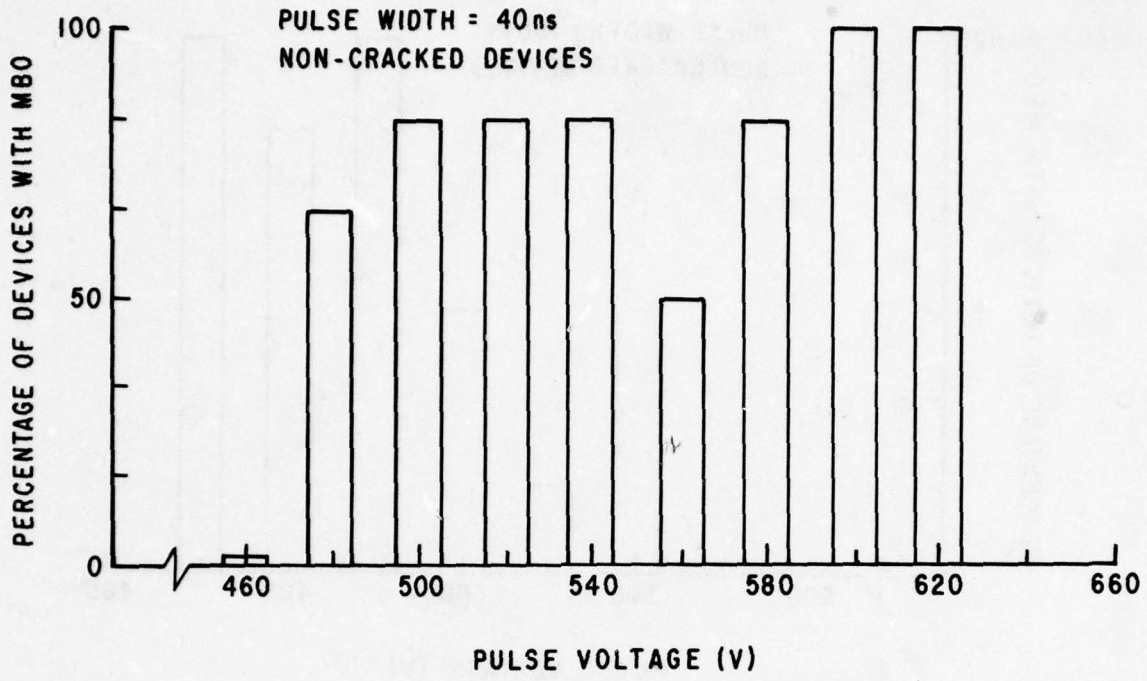


Figure 18. Percentage of burnouts versus pulser voltage, 40 ns, uncracked devices.

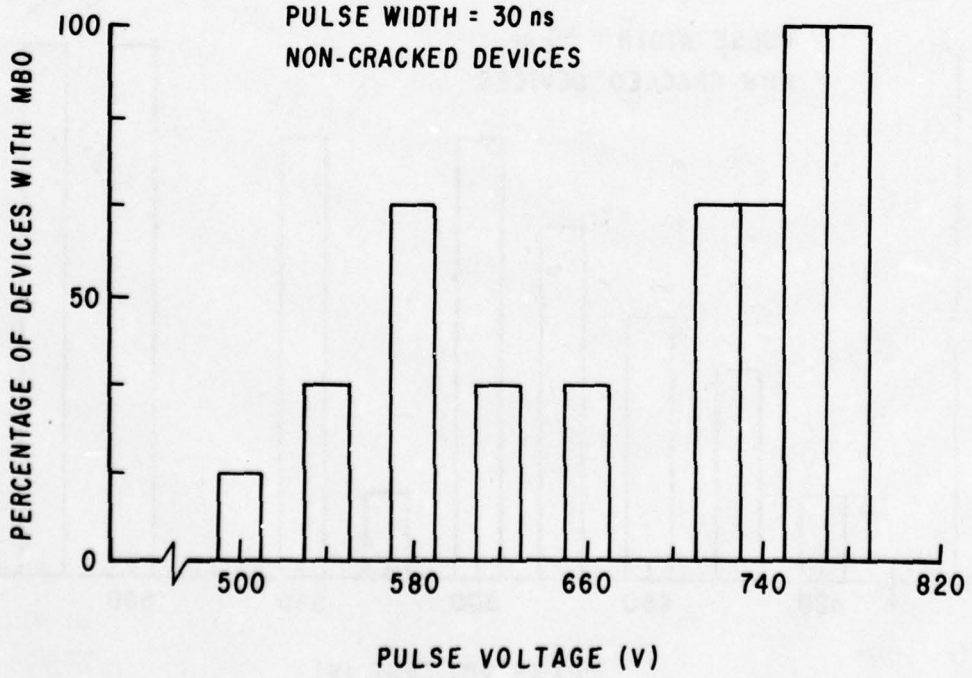


Figure 19. Percentage of burnouts versus pulser voltage, 30 ns, uncracked devices.

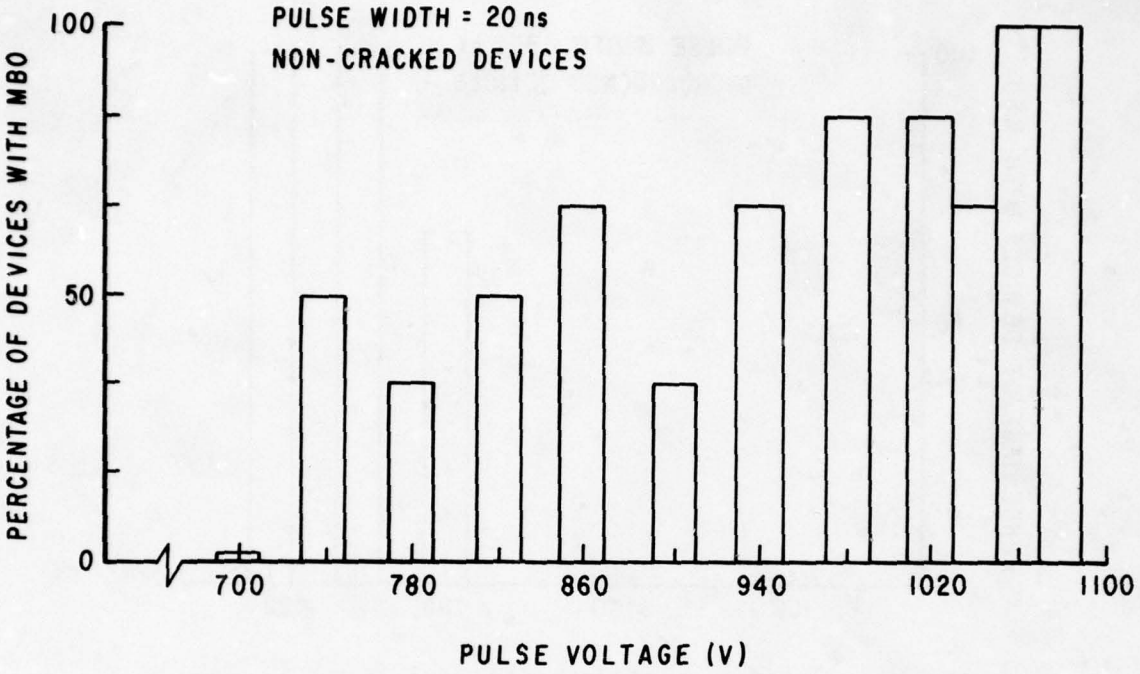


Figure 20. Percentage of burnouts versus pulser voltage, 20 ns, uncracked devices.

threshold can again be seen. Corresponding histograms for the microcracked devices are shown in Figures 21 through 27. For both microcracked and non-microcracked devices, the amplitude of the current was only approximately proportional to the pulser voltage. After the junction breakdown, voltage usually dropped to approximately one-third the selected voltage. To better compare the histograms for all the devices, they have been replotted to include both microcracked and nonmicrocracked devices in Figures 28 through 34. There is some bimodal character to these graphs. The uncracked devices usually displayed MBO at lower voltages than the microcracked devices. In fact, it seemed that the devices might have been labeled incorrectly--all microcracked devices with marks indicating they were not cracked, and vice versa. However, SEM tests did reveal microcracks on the devices so marked, while none appeared on the devices marked as uncracked.

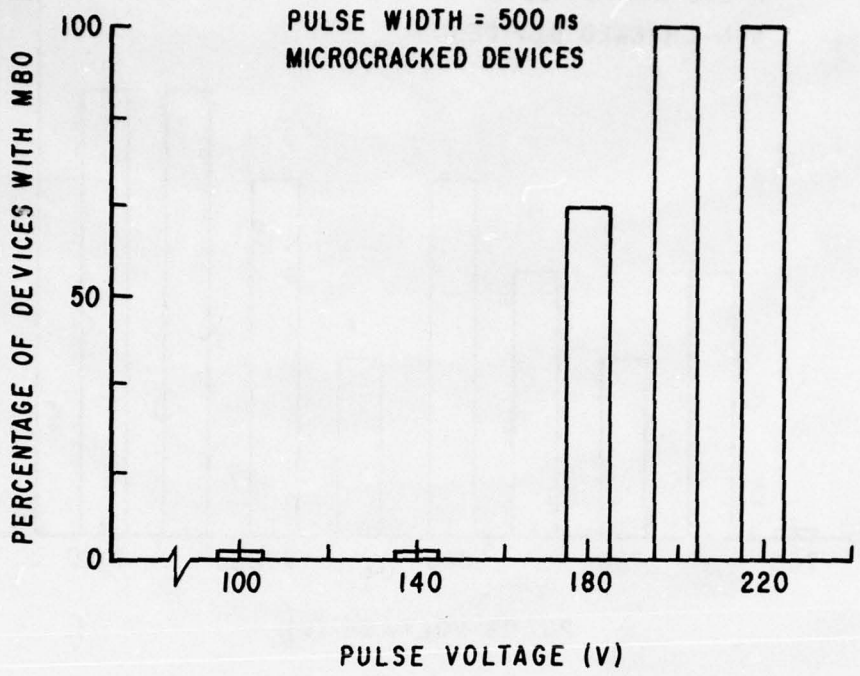


Figure 21. Percentage of burnouts versus pulser voltage, 500 ns, microcracked devices.

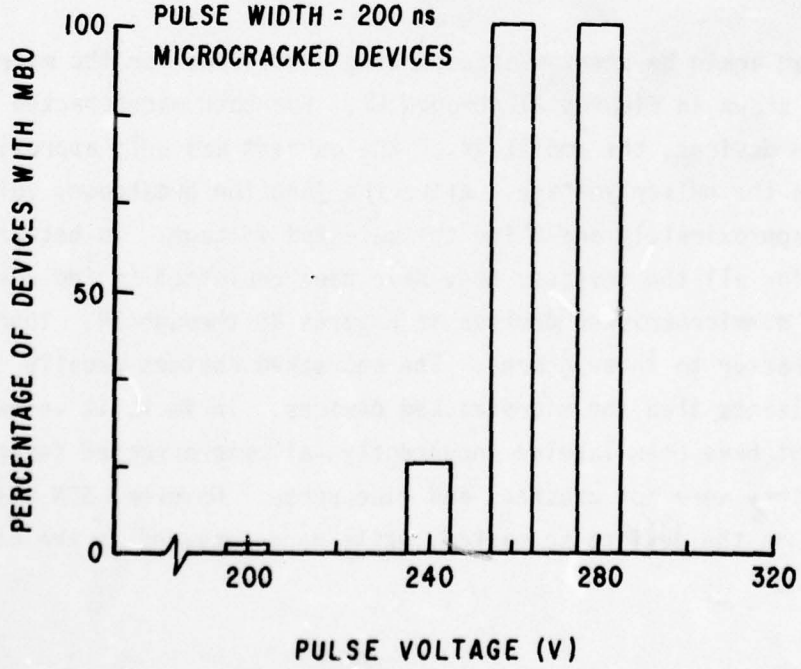


Figure 22. Percentage of burnouts versus pulser voltage, 200 ns, microcracked devices.

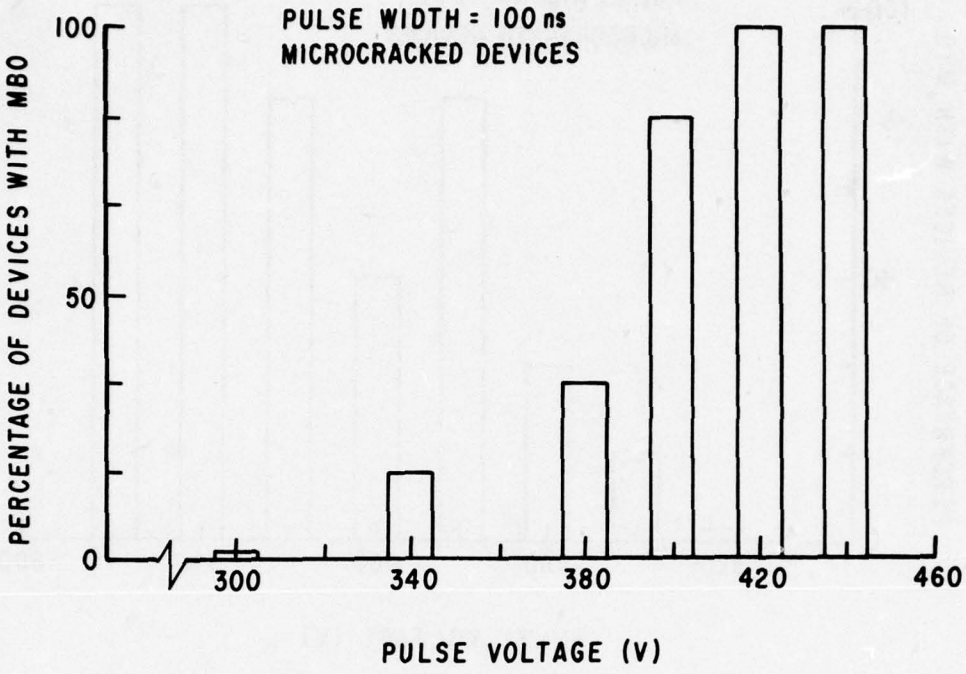


Figure 23. Percentage of burnouts versus pulser voltage, 100 ns, microcracked devices.

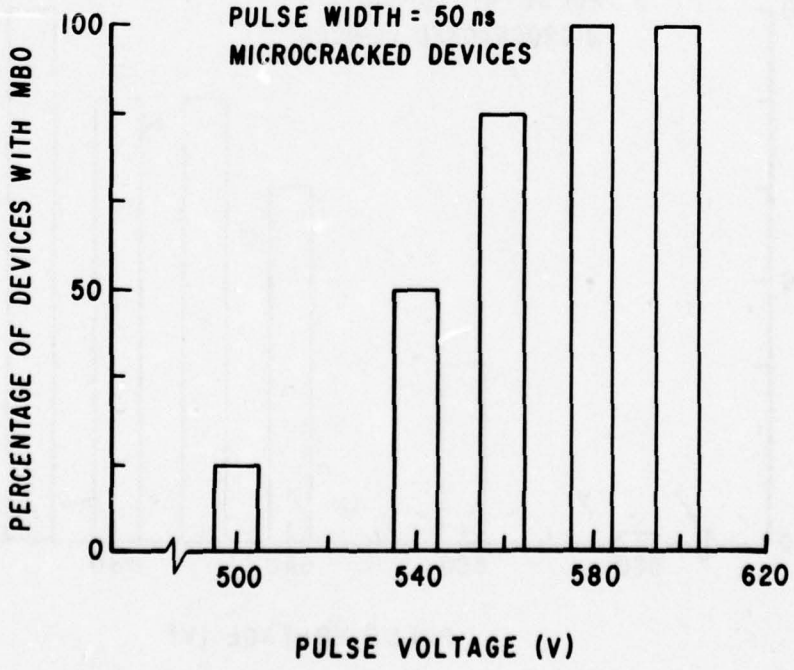


Figure 24. Percentage of burnouts versus pulser voltage, 50 ns, microcracked devices.

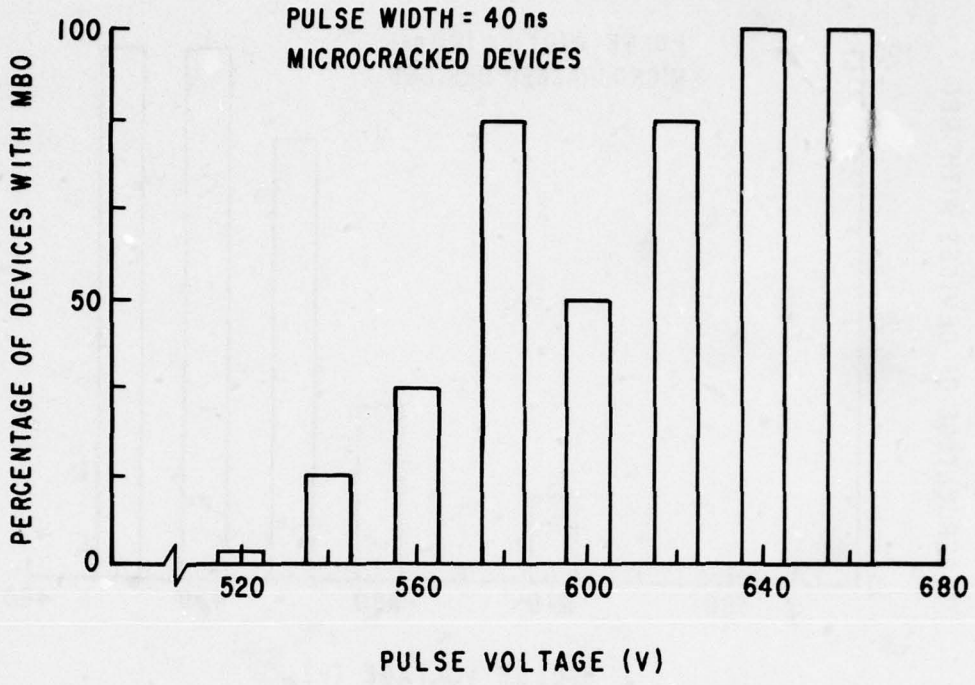


Figure 25. Percentage of burnouts versus pulser voltage, 40 ns, microcracked devices.

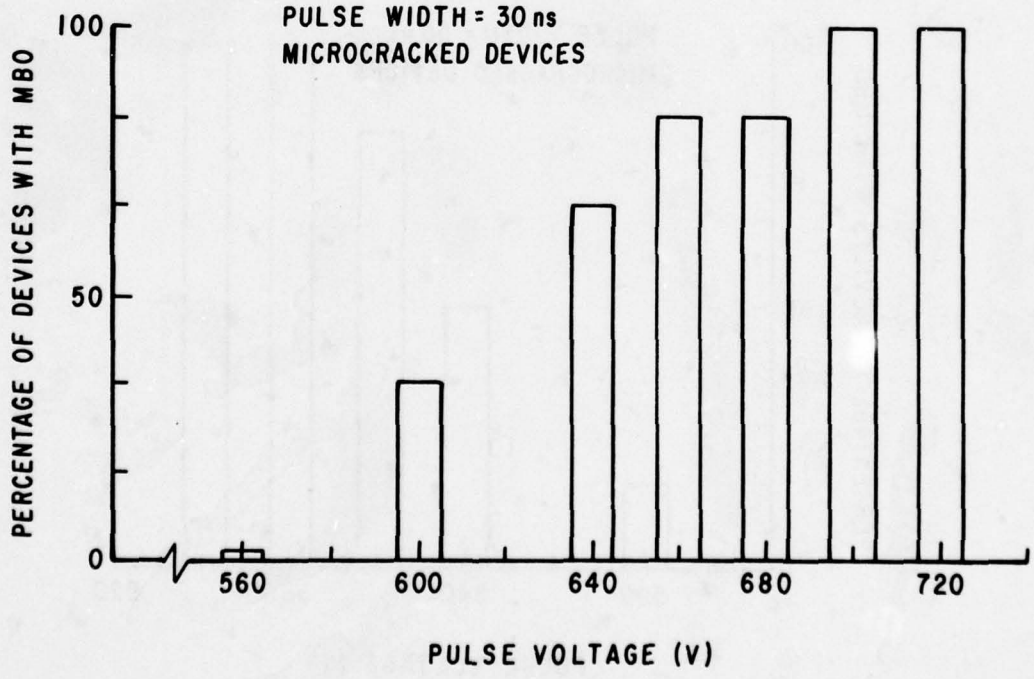


Figure 26. Percentage of burnouts versus pulser voltage, 30 ns, microcracked devices.

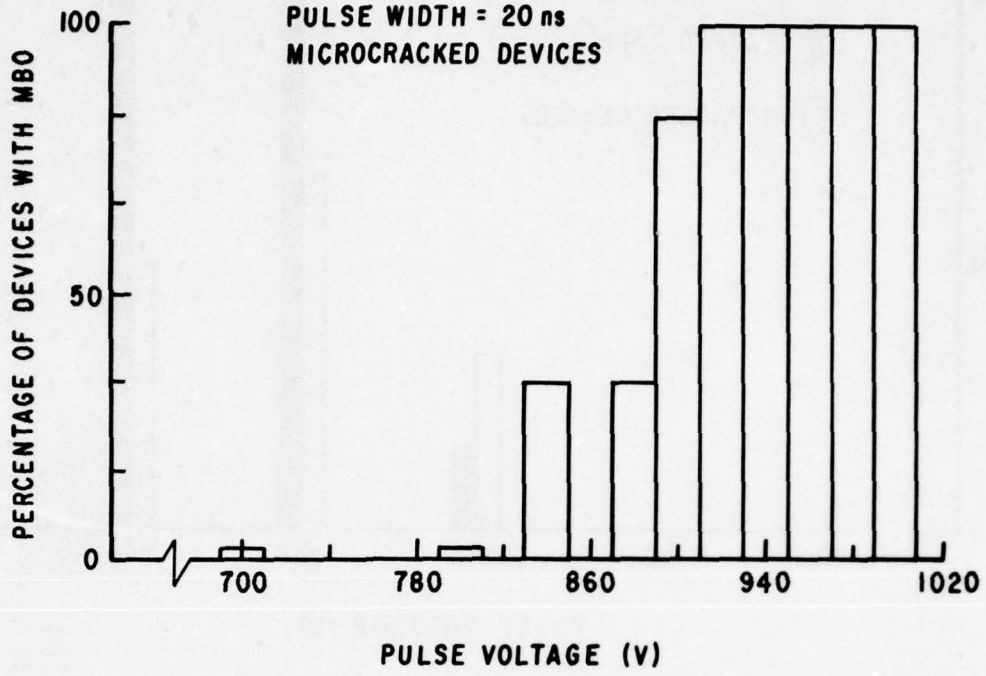


Figure 27. Percentage of burnouts versus pulser voltage, 20 ns, microcracked devices.

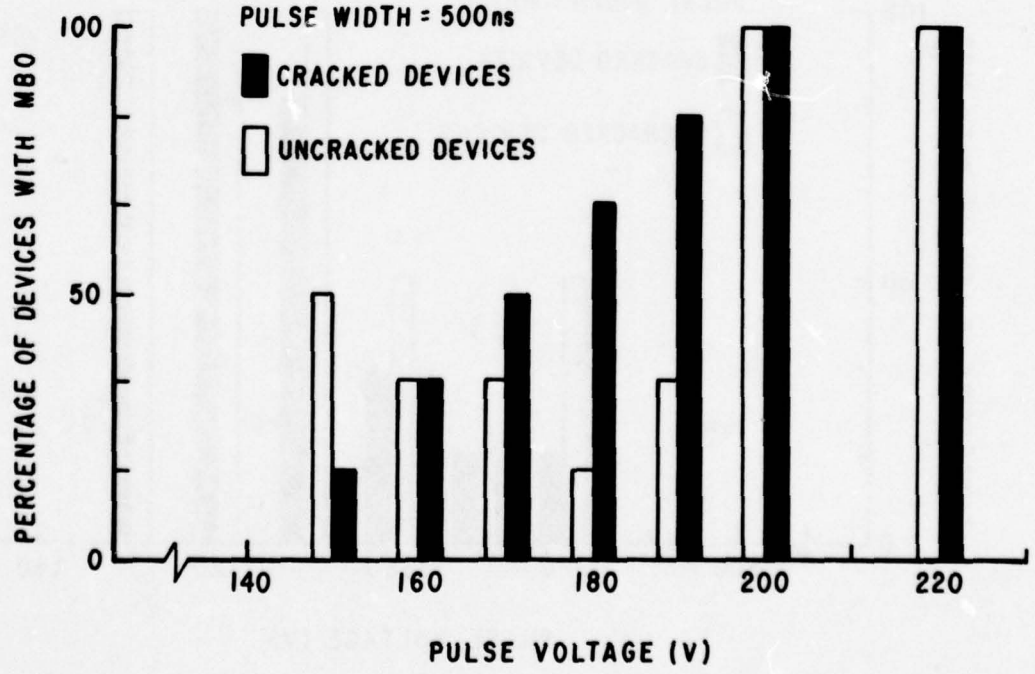


Figure 28. Comparison of uncracked and microcracked devices, 500 ns pulse.

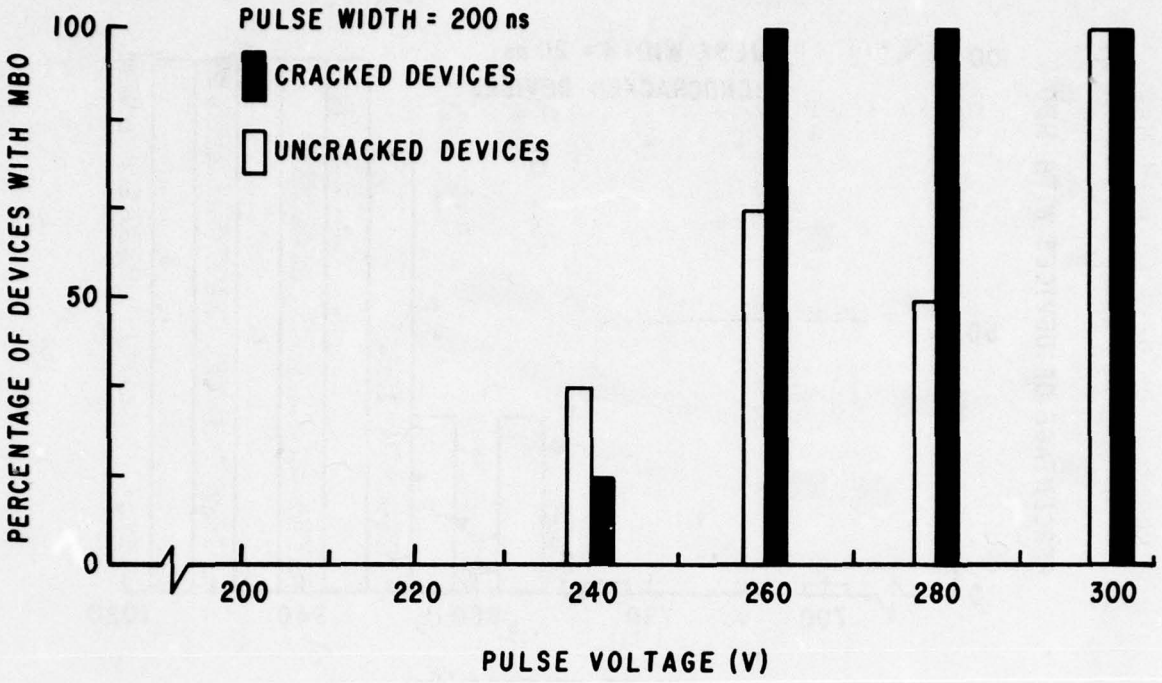


Figure 29. Comparison of uncracked and microcracked devices, 200 ns pulse.

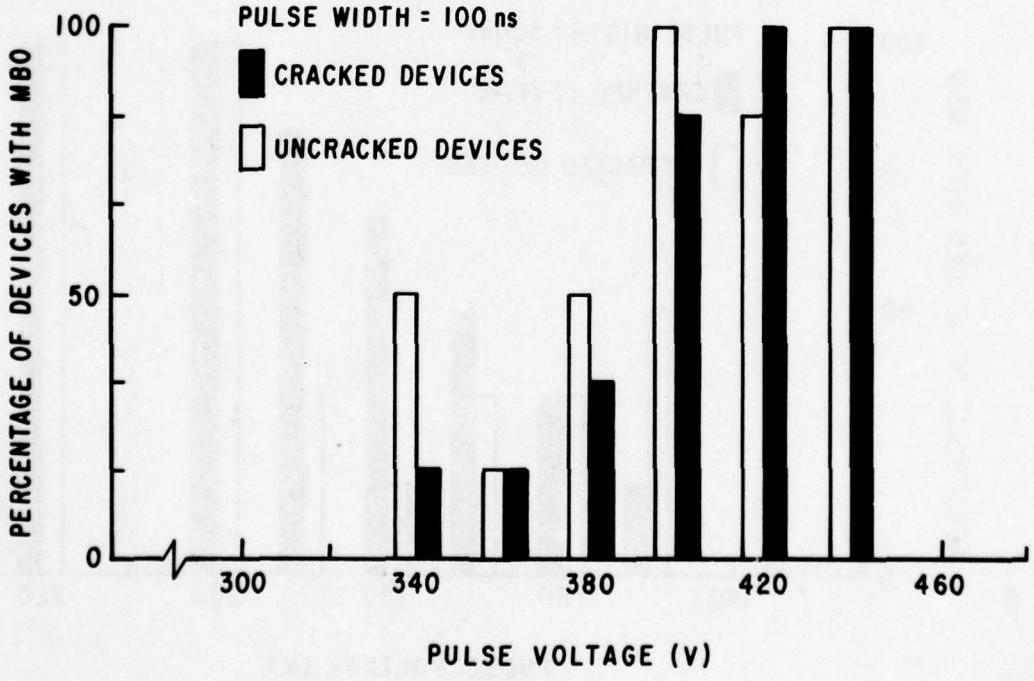


Figure 30. Comparison of uncracked and microcracked devices, 100 ns pulse.

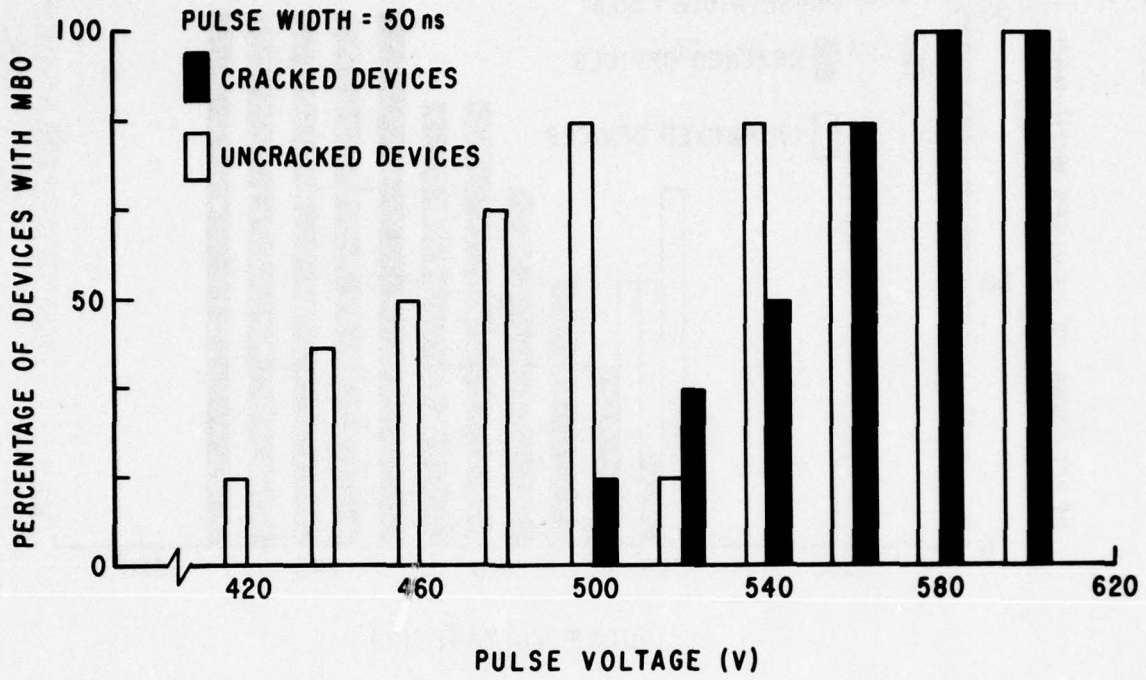


Figure 31. Comparison of uncracked and microcracked devices, 50 ns pulse.

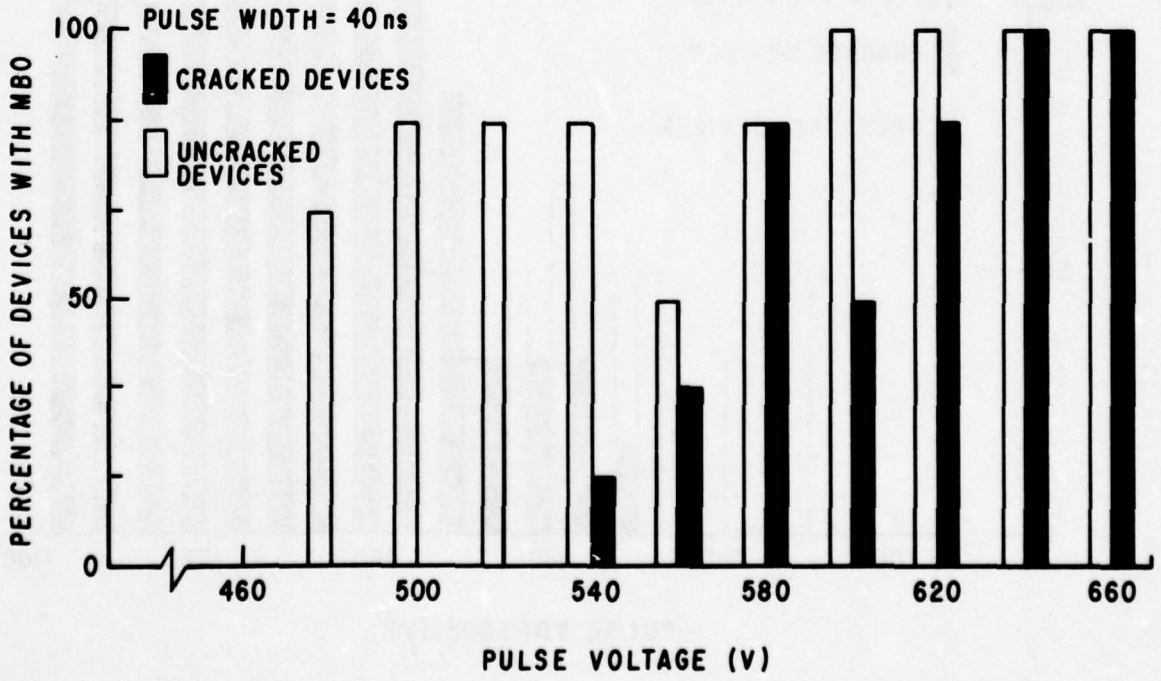


Figure 32. Comparison of uncracked and microcracked devices, 40 ns pulse.

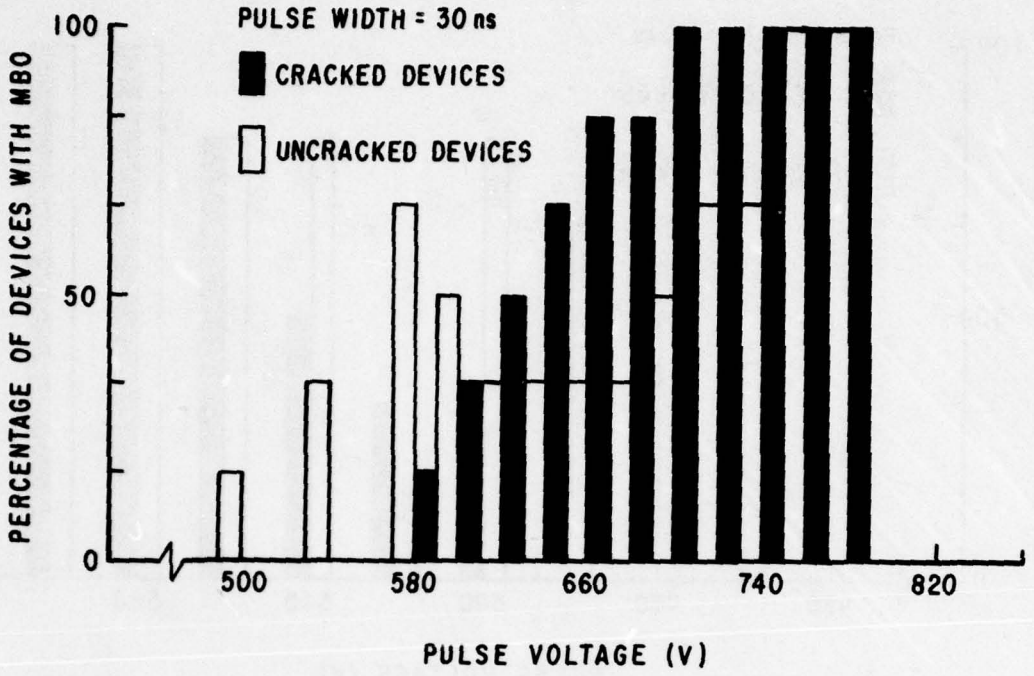


Figure 33. Comparison of uncracked and microcracked devices, 30 ns pulse.

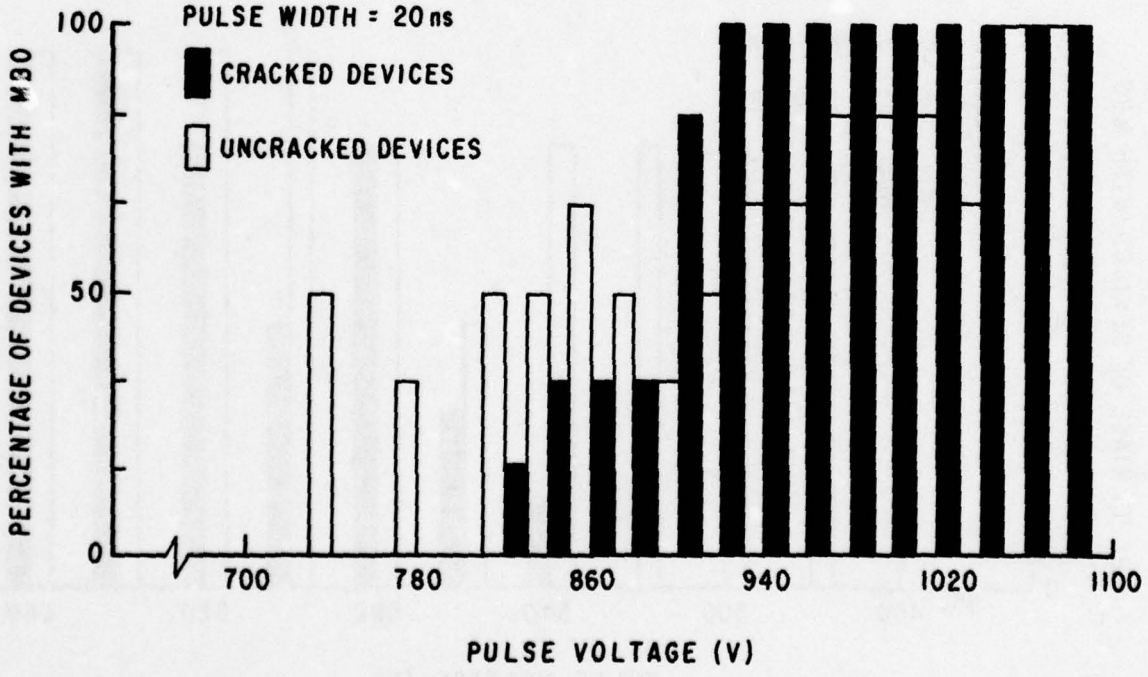


Figure 34. Comparison of uncracked and microcracked devices, 20 ns pulse.

ANALYSIS

The histograms of burnout versus pulse voltage offered some puzzling results. However, the important parameter in these studies was actually the current flowing through the metallization. Fortunately, the oscillographs recorded for each pulse allowed a determination of burnout versus current. Due in part to differences in resistance between devices, the amplitude of the current was not fixed for a given pulser voltage. Therefore, each oscillograph was examined to determine the current seen by the metallization. A potential problem was encountered in graphically representing the data. The burnout versus voltage histograms were constructed using the percentage of devices burned out at each given voltage. Since an equal number of devices were tested at each voltage, there was no problem in weighting of the results. However, since the current was not fixed with respect to the voltage, the number of devices tested at an arbitrary current varied widely. A possible choice for the vertical axis of the current histograms was the actual number of devices burned out at a given current. (Otherwise, one device might burn out at a lower current and, if it was the only device tested at that current, would show up on the histogram as 100 percent burnout, whereas six devices out of ten at a higher current would show only 60 percent burnout.) A further modification of this idea was the eventual choice for the burnout-current histograms. The total number of burnouts for the pulse width in question was determined; the height of the bars was then set equal to the percentage of the burnouts occurring at a given current. This choice of plots yielded a histogram nearly identical to the one which would have been generated by plotting actual numbers versus current, but normalized to the total number of burnouts. This allowed comparison between two or more of these histograms. Figures 35 through 41 are the histograms constructed using this method; each pair of histograms shows the results for a particular pulse width for both uncracked and microcracked devices.

These histograms show the microcracked devices burn out at higher currents than the uncracked devices, though there is significant overlap of the ranges in which burnout occurs. However, one final correction is necessary. As previously mentioned, the thickness of the emitter metallization on the uncracked and microcracked devices was 1.9 μm and 1.4 μm, respectively. In addition, the widths of the metallization also differed. The average width of the uncracked emitter metallization was 8 μm, while for the microcracked devices, this width

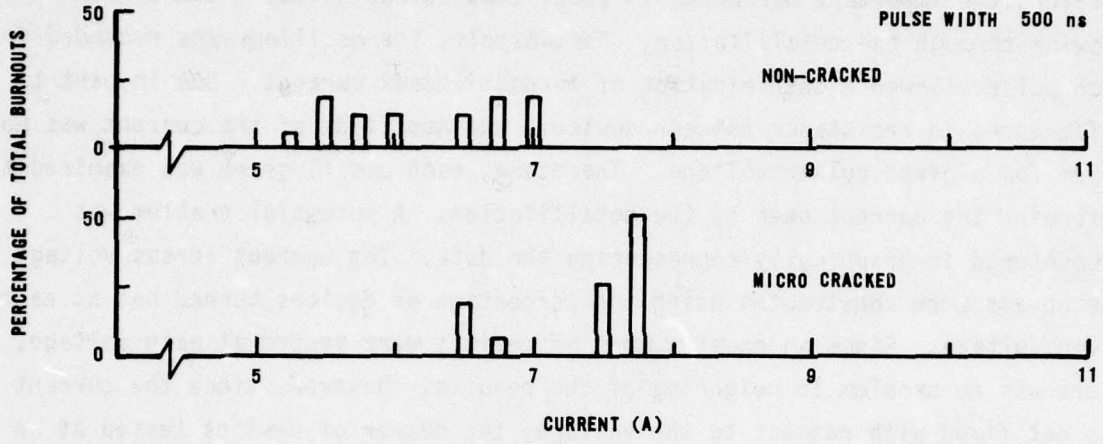


Figure 35. Burnout versus current, 500 ns pulse.

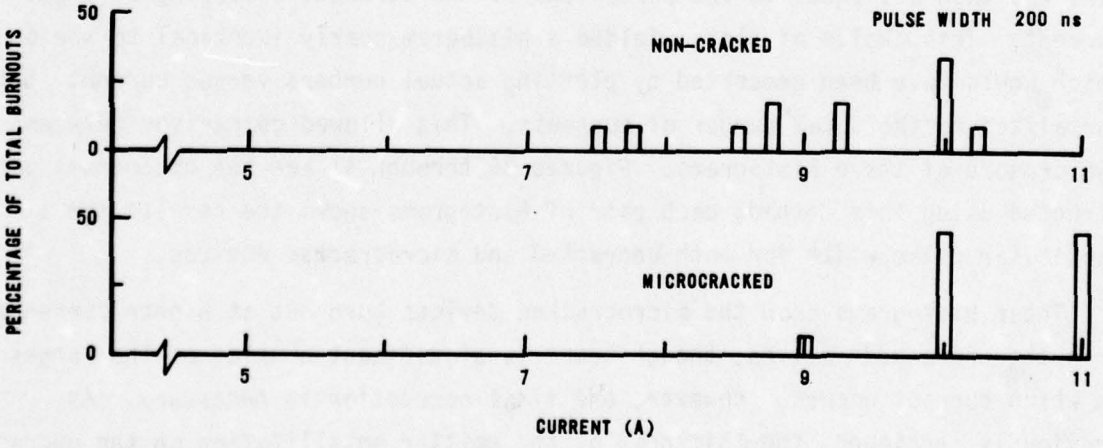


Figure 36. Burnout versus current, 200 ns pulse.

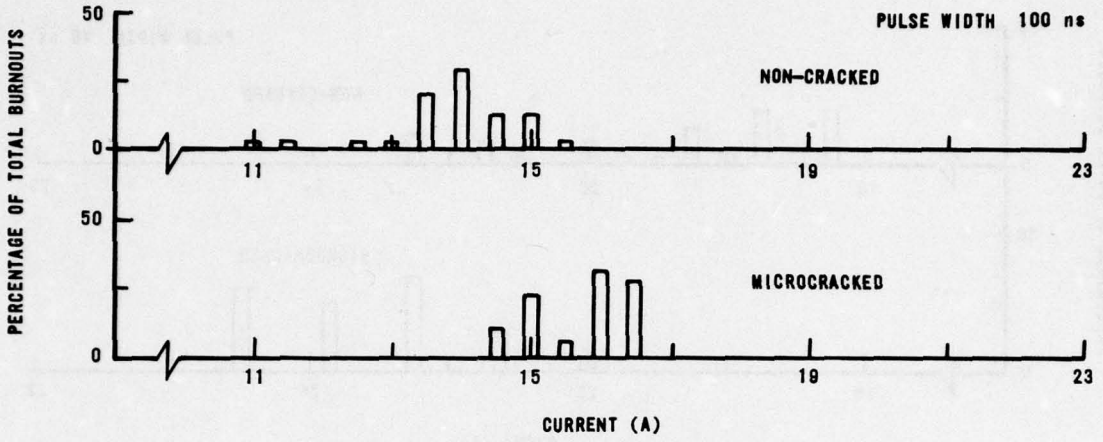


Figure 37. Burnout versus current, 100 ns pulse.

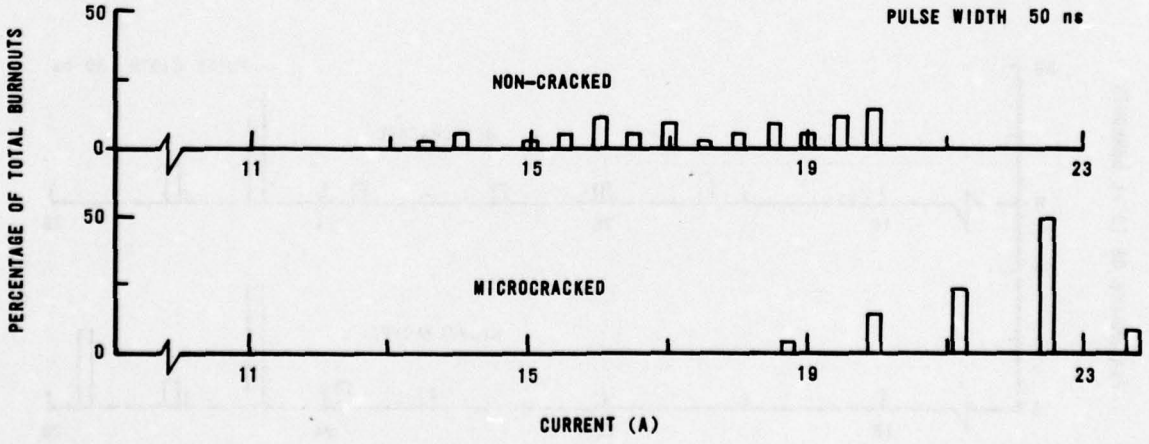


Figure 38. Burnout versus current, 50 ns pulse.

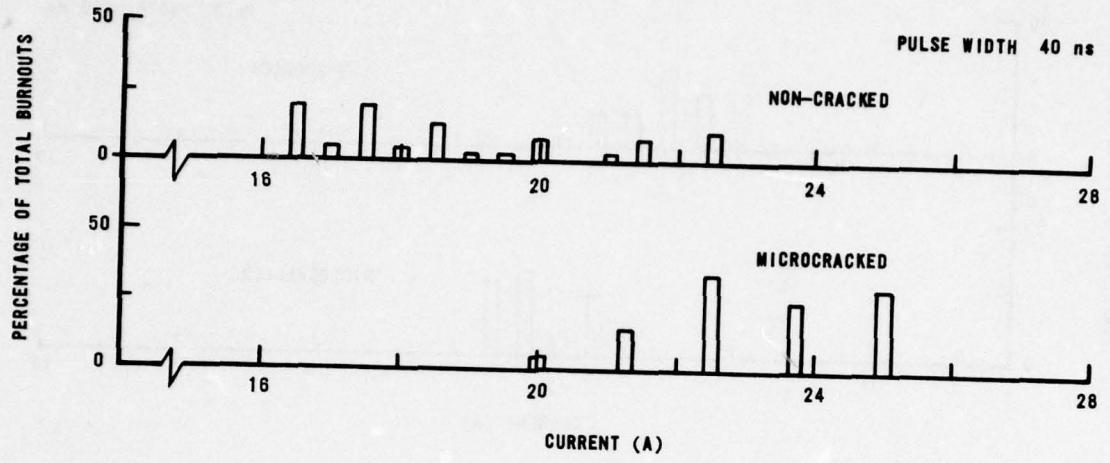


Figure 39. Burnout versus current, 40 ns pulse.

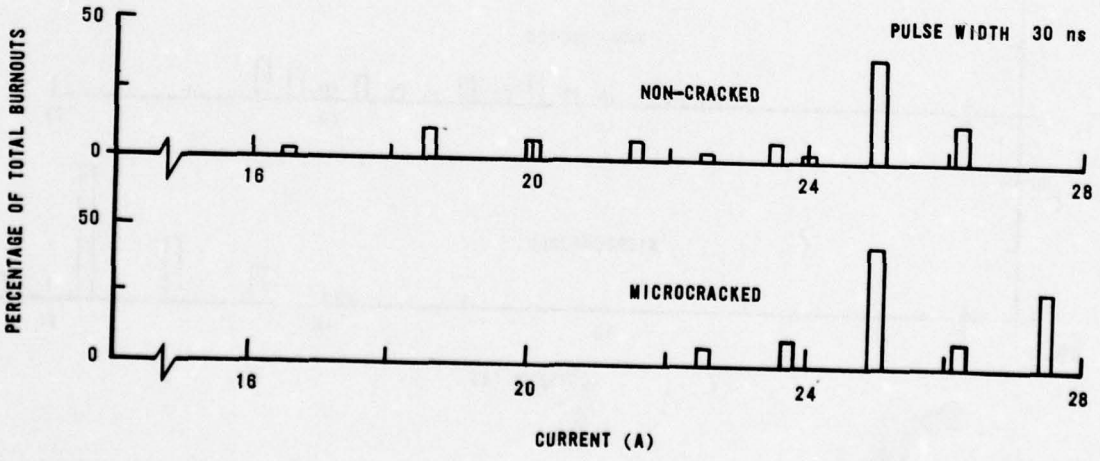


Figure 40. Burnout versus current, 30 ns pulse.

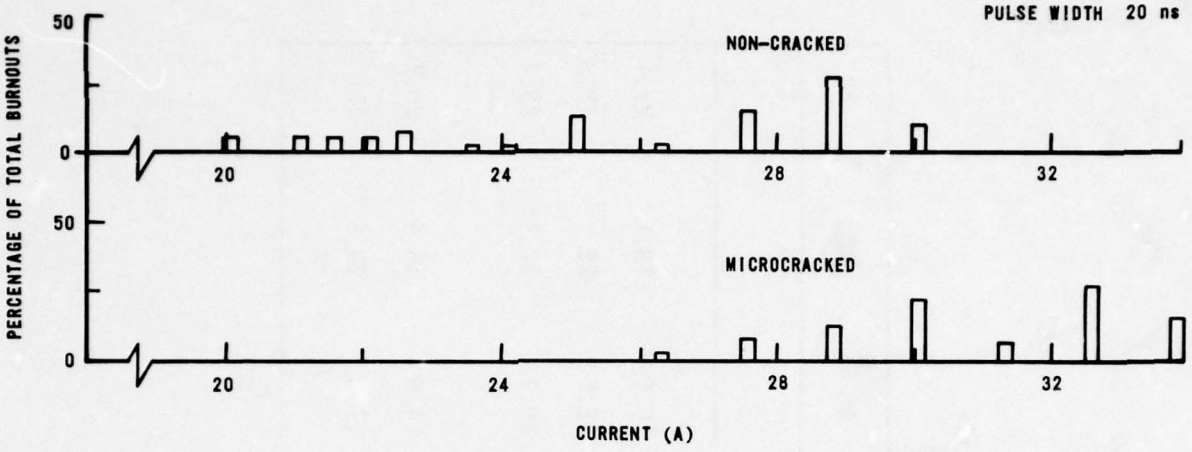


Figure 41. Burnout versus current, 20 ns pulse.

was approximately 12 μm. The width varied from device to device, with as much as 20 percent deviation for the most drastic differences. The average cross sections over field oxide for the uncracked and microcracked devices were thus 1.5×10^{-7} and 1.7×10^{-7} cm^2, respectively. To correctly compare the two sets of burnout data therefore requires a correction for these cross sections.

Using Equation 10, assuming adiabatic conditions, the current required for melting of the metallization should be

$$I = (1.95 \times 10^4)\, At^{-\frac{1}{2}}$$

The microcracked current levels would thus have to be reduced by the ratio of the uncracked to microcracked cross sections to compare the burnout levels. This ratio is approximately 0.88. After this correction, the burnout currents for the two sets of devices are quite similar.

The theoretical melting currents for each pulse width are shown in Table 8. The calculated current is shown for both microcracked and uncracked devices. To compare the theory and experiment, an artifact of the experimental procedure had to be taken into account. For each pulse width, a voltage was found at which all devices tested exhibited burnout. However, one or more higher voltage

TABLE 9. THEORETICAL AND EXPERIMENTAL BURNOUT CURRENTS

Pulse Width (ns)		500	200	100	50	40	30	20
Device	Method	Current (A)						
Microcracked	Theory	4.7	7.4	10.5	14.8	16.6	19.1	23.4
	Experiment	7.5	10	15	21.3	22.5	25	28.8
	Corrected	6.6	8.8	13.2	18.8	19.9	22.1	25.4
Uncracked	Theory	4.1	6.5	9.2	13.1	14.6	16.9	20.7
	Experiment	6.0	9.3	13.5	17	17.5	23.5	25

pulses were usually used to verify this 100 percent burnout level. These higher level pulses (also having higher currents) caused some weighting of the burnout versus current histograms. In calculating a mean burnout current, these extra data points would shift the mean upwards. After correcting for these points (by ignoring their presence), a mean value was found for each pulse width for both the microcracked and uncracked devices. These weighted values appear in Table 9 in the "Experiment" rows. Finally, the mean currents for the microcracked devices are shown after correcting for the cross-section ratio, to allow comparison with the uncracked means.

In general, the cracked and uncracked mean burnout currents agree within 10 percent after the cross-section correction. However, there is considerable disagreement between the calculated and experimental currents. Several factors probably contribute the bulk of this discrepancy. One of these could be the use of the mean current, rather than the minimum. However, it was felt that the mean value more truly represents the burnout current, and that lower (or higher) currents are at least partly due to variations in cross section. The second possibility is that a substantial amount of extra current is required beyond melting before MBO occurs. This may be necessary to initiate pulling back of the molten aluminum to create an open, or may be the result of the energy required for vaporization of the metal. However, previous investigators (Ref. 23) have shown the latter to be negligible. The third factor is probably the most serious. The calculated current is based on a rectangular pulse. The pulses used in this experiment were usually quite unrectangular. Lastly, for the longer pulses (which did approach a rectangular shape), nonadiabatic conditions probably existed. The error is probably due to a combination of these and other factors, with pulse shape playing the primary role.

SECTION IV

CONCLUSIONS

The microcracked devices in this study did not suffer metallization burnout at a level significantly different from the uncracked devices. Metallization generally burned out over field oxide, usually at a point approximately halfway between two areas of lower temperature. Previous studies had suggested that microcrack burnout might not occur because of heat sinking by thinner oxide or the silicon at the window; pulses shorter than the adiabatic limit would be required to cause microcrack burnout. In the tests reported here, short pulses with rapid risetimes were employed in an effort to reach adiabatic conditions. Nevertheless, few microcrack burnouts were induced.

Several explanations are possible for these results. Nonadiabatic conditions may still have existed. Further studies by Gurev (Ref. 28) complementing his work with AFWL indicated that the adiabatic limit was strongly dependent on microcrack shape. Thermal diffusion calculations yielded times shorter than 1 ns as being necessary to approach adiabatic conditions in some cases. However, his experimental results did not confirm his thermal diffusion model, and he found 30 ns to 1 μs pulses could differentiate between good metallization and defective metallization. However, Gurev's work used special metallization stripes, in contrast to the experiments reported here. This avoided many of the problems we encountered with junction effects, resistors, and parallel current paths. However, a true production line test would be on devices such as ours, not on simple stripes. Another possible discrepancy in our experiment was the large difference in emitter and collector cross sections. The problem of mismatched cross sections on a real device (such as the emitter-collector ratio of 1:30 for the output transistor) may represent an insurmountable testing problem. Attempts to pulse devices which had more equal cross sections were difficult in this experiment. For components made today, consisting of hundreds or thousands of active elements, the testing of a single transistor (or even a few) would be extremely difficult, involving multiple current paths and analysis of numerous possible logic states.

Burnout of junctions presents another problem for testing of devices. For most of the devices pulsed in this experiment, junction burnout occurred at lower currents than did metallization burnout. Hence, nonmicrocracked devices

would not survive a screen of this type. Only at very short pulse lengths (< 20 ns) did a significant number of devices survive electrically even when MBO did not occur.

If a manufacturer included special test stripes on the chip, pulse testing might be feasible. However, the amount of room required for the stripes would be prohibitive on a chip already crowded with devices. In addition, the pads required for testing these stripes would require additional room, and would further complicate the already complex problem of packaging components that use many input and output leads.

Therefore, the primary conclusion of this report is that production line tests using current pulses do not represent a viable microcrack screening technique. In addition, with the increasing density of elements on a chip, the SEM may also become inadequate. This would leave no screening technique at all.

Fortunately, evidence seems to indicate that as IC technology has matured, the problem of microcracks has decreased. Literature on reliability has included little on microcracks in the past few years. In fact, the proceedings of the annual IEEE Reliability Physics Symposium, which published the majority of microcrack articles, have not included a paper on microcracks since 1974. Several factors have contributed to the lessening of microcrack problems. Tapering of steps and contact window edges can be performed by controlled chemical processing (Ref. 29). Elevated substrate temperature during deposition of the metallization layer and nutation of the wafer can provide more uniform coverage (Ref. 30). Improvements in deposition hardware (such as planetary wafer holders) and techniques (such as sputtering) have also helped eliminate microcracks (Ref. 31).

The possibility of MBO in nuclear environments is still present and cannot be easily eliminated. However, microcracks should not play a role in this radiation effect. The microcrack as a reliability and nuclear vulnerability problem now appears to be minimal. This should continue as long as microelectronics processing technology continues to meet and maintain present standards.

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